JFET Input Operational Amplifier - TL072M

Low-Noise JFET Input Operational Amplifier in bare die form

Rev 1.0
14/02/19

Description

The TL072M dual operational amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip. This combination delivers low input bias and offset currents with fast slew rates. Low harmonic distortion and low noise provide high quality amplification for use in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other general purpose circuits. A low offset voltage temperature coefficient enables performance across the full military temperature range.

Features:

- Low Noise e_n = 15nV/√Hz (typ)
- Low Harmonic Distortion : 0.003% (typ)
- Wide Common-Mode (to V_{CC}+) & Differential Voltage ranges
- Low Input Bias and Offset Currents
- High Slew Rate: 16V/µs(typ)
- High Input Impedance JFET-Input Stage
- Short-Circuit Protection & Latch-Up Free Operation

Ordering Information

The following part suffixes apply:

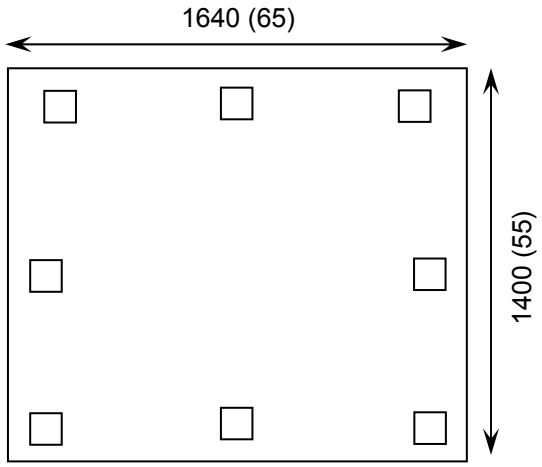
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1640 x 1400 65 x 55	µm mils
Minimum Bond Pad Size	110 x 110 4.33 x 4.33	µm mils
Die Thickness	280 (±20) 11.02 (±0.79)	µm mils
Top Metal Composition	Al-Si-Cu 3.3 µm	
Back Metal Composition	N/A – Bare Si	

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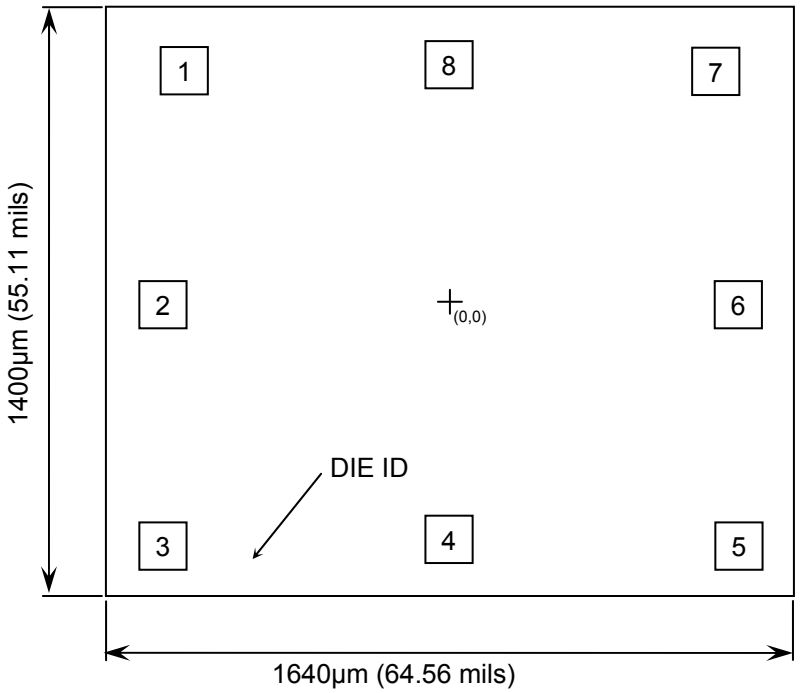
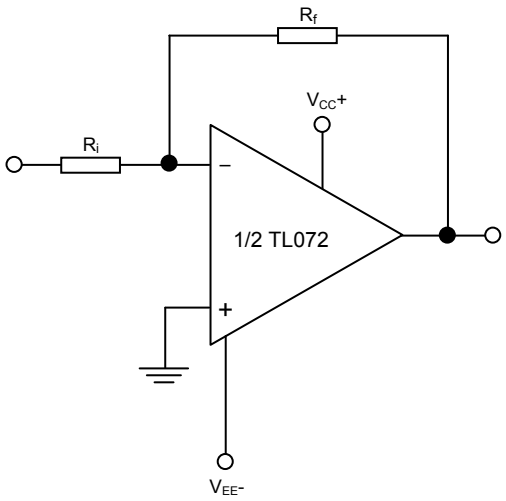
Pad Layout and Functions

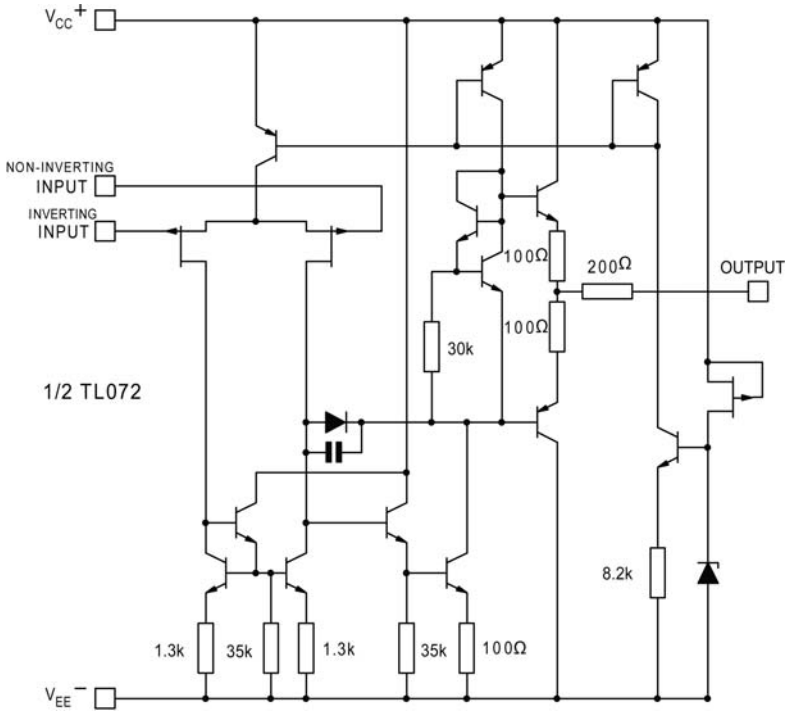


PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	OUTPUT	-0.634	0.567
2	-INPUT	-0.685	-0.034
3	+INPUT	-0.686	-0.578
4	V_{EE}	0	0.565
5	+INPUT	0.686	-0.578
6	-INPUT	0.685	-0.034
7	OUTPUT	0.634	0.567
8	V_{CC}	0	0.578
CHIP BACK POTENTIAL IS FLOAT			

Typical connection



Device Schematic



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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC} ,V_{EE}	±18	V
DC Input Voltage Range (Referenced to GND)[2]	V_{IDR}	±15	V
DC Differential Input Range Voltage[3]	V_{ID}	±30	V
Output Short Circuit Duration	t_{SC}	Continuous	
Power Dissipation in Still Air	P_D	680	mW
Storage Temperature Range	T_{STG}	-65 to +150	°C
Operating Temperature Range	T_J	-55 to +125	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15V, whichever is less. **3.** Differential voltages are at INPUT+, with respect to INPUT− **4.** The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage[5]	V_{CC}	5	15	V
	V_{EE}	-5	-15	
Common-mode voltage	V_{CM}	V_{EE} +4	V_{CC}	V
Operating Temperature Range	T_J	-55	+125	°C

5. V_{CC} and V_{EE} are not required to be of equal magnitude, provided that the total supply (V_{CC} – V_{EE}) is between 10V and 30V.

Electrical Characteristics (V_{CC} = 15V, V_{EE} = -15V, T_J = -55°C to +125°C unless specified otherwise)

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Input offset voltage	V_{IO}	R_S = 50Ω, V_O = 0	T_J = 25°C	-	3	6	mV
			T_J = Full range	-	-	9	
Temperature coefficient of input offset voltage	ΔV_{IO}	R_S = 50Ω, V_O = 0	T_J = Full range	-	18	-	µV/°C
Input offset current[6]	I_{IO}	V_O = 0	T_J = 25°C	-	5	100	pA
			T_J = Full range	-	-	20	nA
Input bias current[6]	I_{IB}	V_O = 0	T_J = 25°C	-	20	200	pA
			T_J = Full range	-	-	50	nA
Common-mode input voltage range	V_{ICR}			±11	-12 to +15	-	V
Maximum peak output voltage swing	V_{OM}	R_L = 10kΩ	T_J = 25°C	±12	±13.5	-	V
		R_L = 2kΩ	T_J = Full range	±10	-	-	
		R_L = 10kΩ	T_J = Full range	±12	-	-	

6. The input bias currents are junction leakage currents which approximately double for every 10°C increase in junction temperature.

Electrical Characteristics (V_{CC} = 15V, V_{EE} = -15V, T_J = -55°C to +125°C unless specified otherwise)

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Large-signal differential voltage gain	A_{VD}	R_L =2kΩ V_O =±10V	T_J = 25°C	35	200	-	V/mV
			T_J = Full range	15	-	-	
Gain bandwidth product	GBP	R_L = 10kΩ, C_L = 100pF	T_J = 25°C	2.5	4	-	MHz
Input resistance	R_i			-	10^{12}	-	Ω
Common-mode rejection ratio	CMRR	R_S = 50Ω	T_J = 25°C	80	86	-	dB
Supply-voltage rejection ration	SVR	R_S = 50Ω	T_J = 25°C	80	-	-	dB
Supply current	I_{CC}	No load	T_J = 25°C	-	1.4	2.5	mA
			T_J = Full range	-	-	2.5	
Channel separation	V_{O1} / V_{O2}	A_V = 100	T_J = 25°C	-	120	-	dB
Output short-circuit current	I_{OS}		T_J = 25°C	10	40	60	mA
			T_J = Full range	10	-	60	

Switching Characteristics[7] (V_{CC} = 15V, V_{EE} = -15V, T_J = 25°C unless specified otherwise)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Slew rate	SR	V_{IN} = 10V, R_L = 2kΩ, C_L = 100pF, Unity gain	8	16	-	V/µs
Rise time	t_r	V_{IN} = 20mV, R_L = 2kΩ, C_L = 100pF, Unity gain	-	0.1	-	µs
Rise time over-shoot factor	K_{OV}		-	10	-	%
Equivalent input noise voltage	e_n	R_S = 100Ω, f = 1KHz	-	15	-	nv/√Hz
Total harmonic distortion	THD	$V_{IN(rms)}$ = 6V, f=1kHz, R_L≥2kΩ, A_V =1, R_S ≤1kΩ	-	0.003	-	%
		A_V =20dB, f=1kHz, R_L=2kΩ, C_L=100pF, V_O =2V_{PP}	-	0.01	-	
Phase margin	Φm		-	45	-	Degrees

7. Not production tested in die form, characterized by chip design and tested in package.

Typical Characteristics

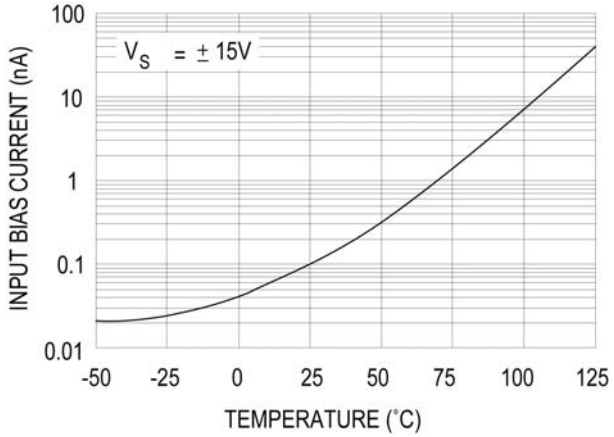

Figure 1 – Input Bias Current vs Temperature

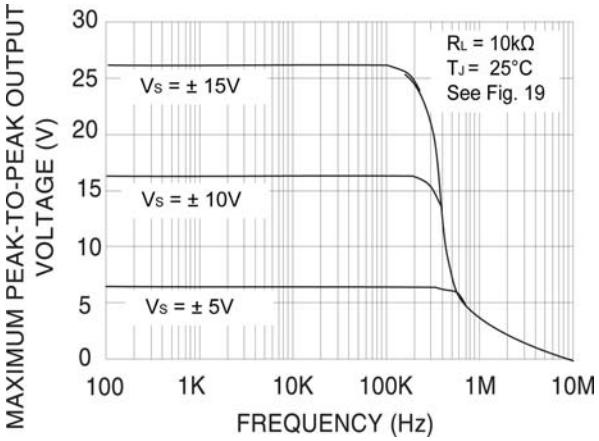

Figure 2 – Maximum Peak-to-Peak output voltage versus Frequency

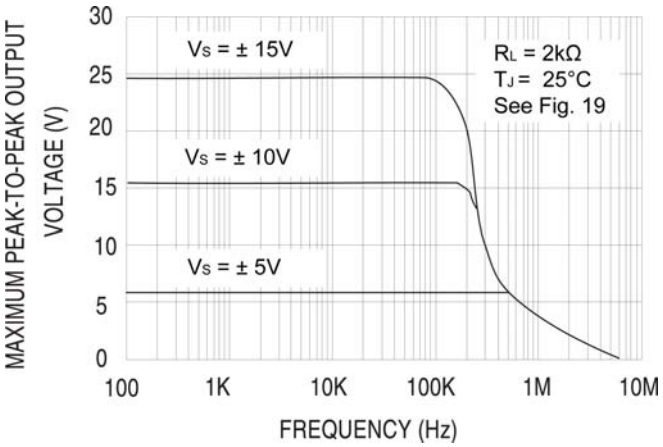

Figure 3 – Maximum Peak-to-Peak output voltage versus Frequency

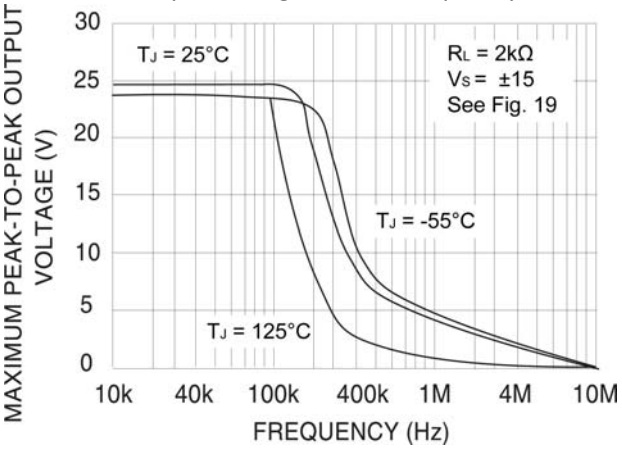

Figure 4 – Maximum Peak-to-Peak output voltage versus Frequency

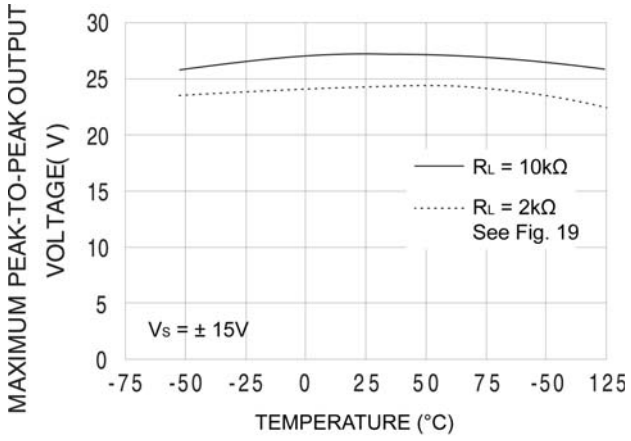

Figure 5 – Maximum Peak-to-Peak output voltage versus Temperature

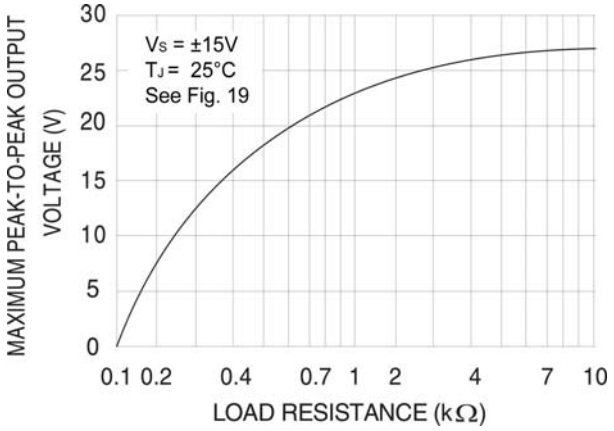

Figure 6 – Maximum Peak-to-Peak output voltage versus Load Resistance

Typical Characteristics

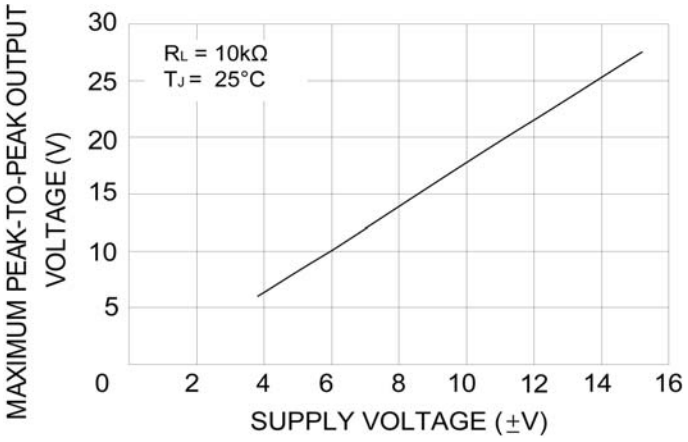

Figure 7 – Maximum Peak-to-Peak Output Voltage versus Supply Voltage

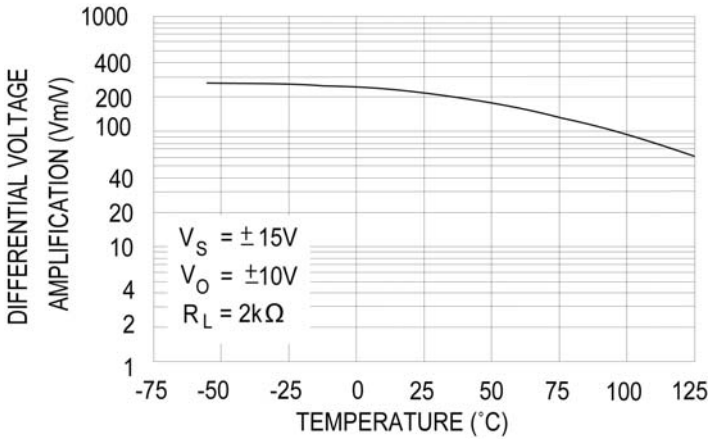

Figure 8 – Large Signal Differential Voltage Amplification versus Temperature

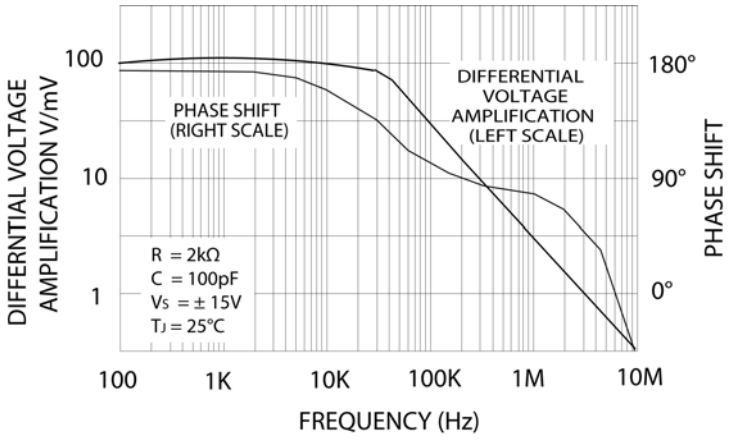

Figure 9 – Large Signal Differential Voltage Amplification & Phase Shift versus Frequency

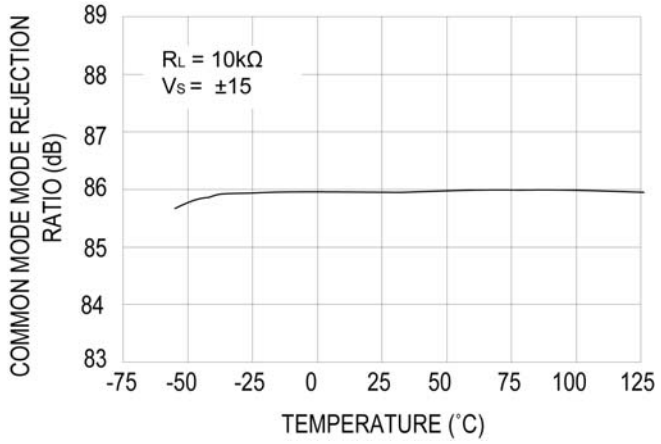

Figure 10 – Common-mode rejection ratio versus Temperature

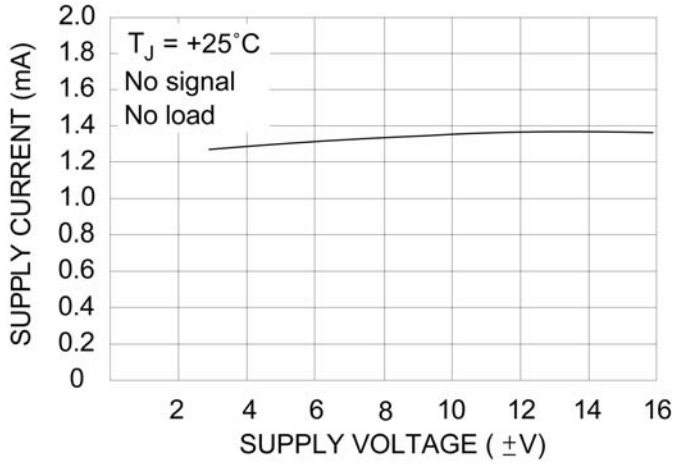

Figure 11 – Supply Current per Channel versus Supply Voltage

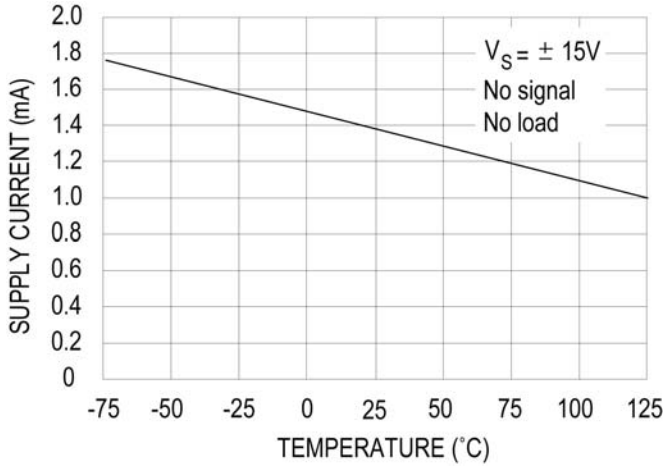

Figure 12 – Supply Current per Channel versus Temp

Typical Characteristics

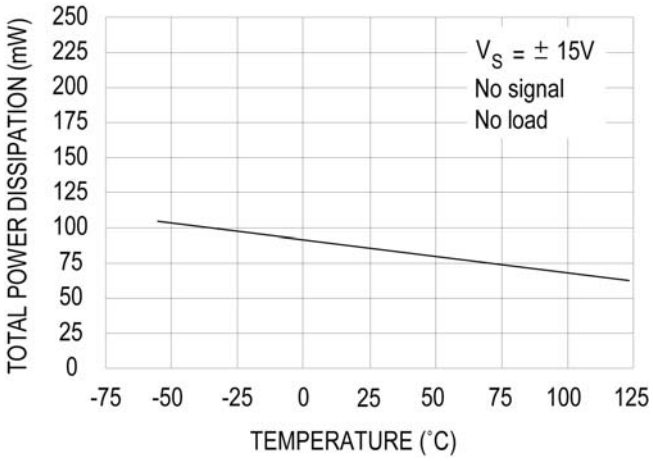

Figure 13 – Total Power Dissipation versus Temperature

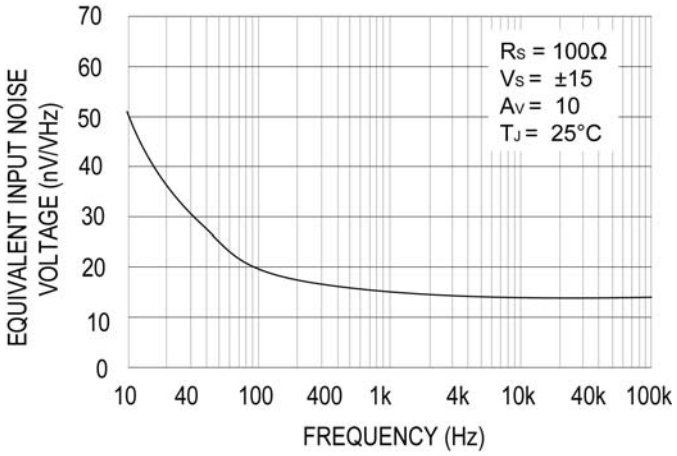

Figure 14 – Equivalent Input Noise Voltage versus Frequency

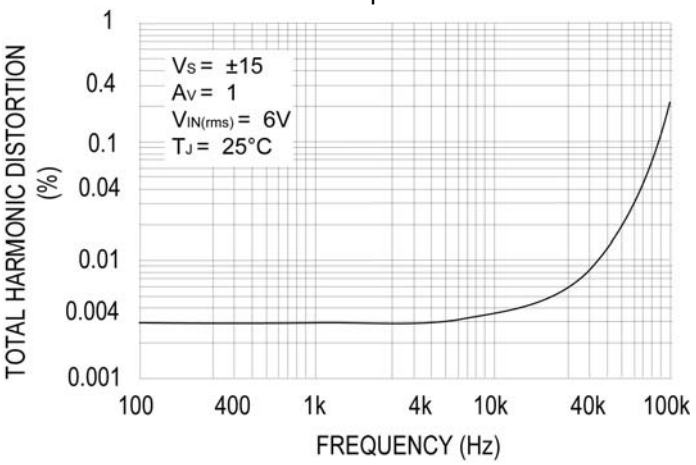

Figure 15 – Total Harmonic Distortion versus Frequency

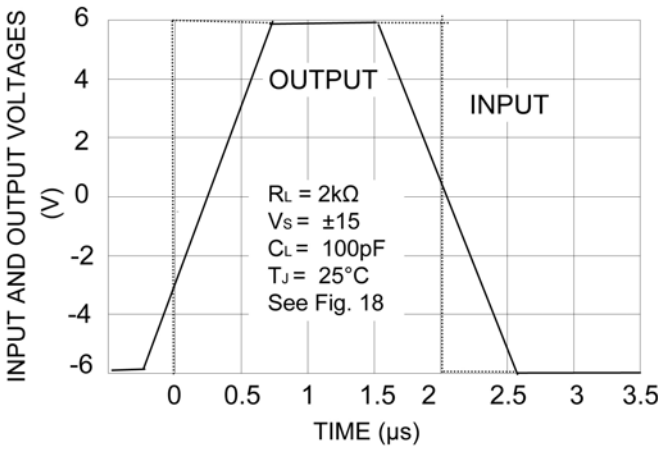

Figure 16 – Voltage follower large-signal pulse response

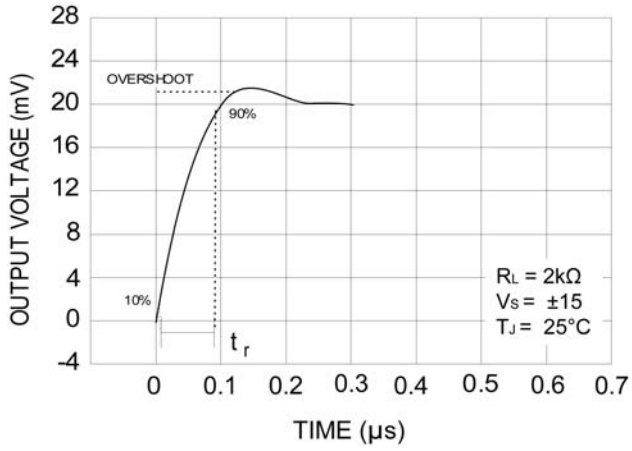

Figure 17 – Output Voltage versus Elapsed Time

Parameter measurement information

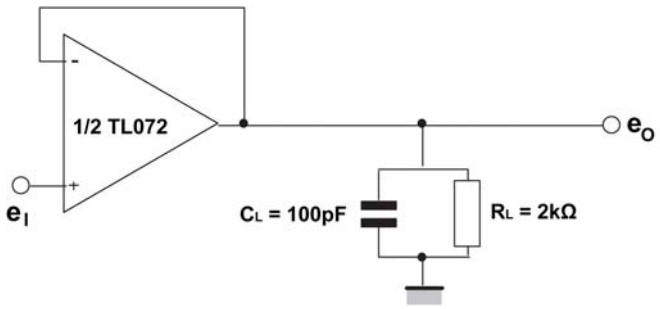

Figure 1 – Voltage Follower

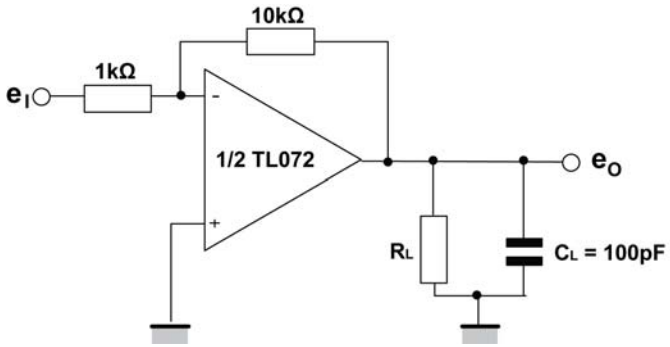

Figure 2 – Gain-of-10 Inverting Amplifier