



# PNP Transistor Bare Die, TIP42C

Rev 1.1  
22/08/23

**Bipolar Medium Power Transistor in bare die form**  
Complement to NPN TIP41C

## Features:

- Collector current up to 6A
- High switching speed
- Improved  $h_{FE}$  linearity
- Solderable back metal
- High Reliability tested grades for Military + Space

## Ordering Information:

The following part suffixes apply:

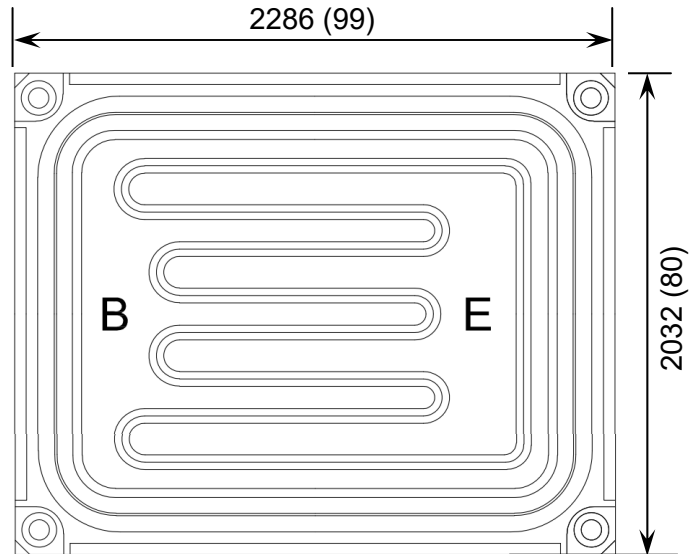
- No suffix - Commercial grade die
- "H" – Hi-rel grade die + MIL-STD-38534 Class H LAT
- "K" – Hi-rel grade die + MIL-STD-38534 Class K LAT.

LAT = Lot acceptance Test.

For information on Hi-Rel LAT flows please see below.

[www.siliconsupplies.com/bare-die-lot-qualification](http://www.siliconsupplies.com/bare-die-lot-qualification)

## Die Dimensions in $\mu\text{m}$ (mils)



**DIE BACK = COLLECTOR**

## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – Specific request
- Unsawn Wafer – Specific request
- With additional electrical selection – Specific request
- Sawn as pairs or adjacent pair pick – Specific request

## Mechanical Specification

Die Size (Excluding Saw Street)	2286 x 2032 99 x 80	$\mu\text{m}$ mils
Base Pad Size Emitter Pad Size	12.5 x 42 13 x 48	mils
Die Thickness	318 ( $\pm 25$ ) 12.5 ( $\pm 1$ )	$\mu\text{m}$ mils
Top Metal Composition	Al	
Back Metal Composition	Ti/Ni/Ag	





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## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	$V_{CBO}$	100	V
Collector-Emitter Voltage	$V_{CEO}$	100	V
Emitter-Base Voltage	$V_{EBO}$	5	V
Collector Current - Continuous	$I_C$	6	A
Collector Current – Peak ( $t_P < 5\text{ms}$ )	$I_{CM}$	10	
Base Current	$I_B$	3	A
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_E = 0$	100	-	-	V
Collector-Emitter Sustaining Voltage <sup>1</sup>	$V_{CEO(SUS)}$	$I_B = 0, I_C = 30\text{mA}$	100	-	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 0$	5	-	-	V
Collector Cut-off Current	$I_{CEO}$	$V_{CE} = 60\text{V}, I_B = 0$	-	-	0.7	mA
Emitter Cut-off Current	$I_{EBO}$	$V_{EB} = 5\text{V}, I_C = 0$	-	-	1	mA
Collector Cut-off Current	$I_{CES}$	$V_{CE} = 100\text{V}, V_{EB} = 0$	-	-	0.4	mA
<b>ON CHARACTERISTICS</b>						
Forward-Current Transfer Ratio <sup>1</sup>	$h_{FE}$	$I_C = 0.3\text{A}, V_{CE} = 4\text{V}$	30	-	-	-
		$I_C = 3.0\text{A}, V_{CE} = 4\text{V}$	15	-	75	-
Collector-Emitter Saturation Voltage <sup>1</sup>	$V_{CE(sat)}$	$I_C = 6\text{A}, I_B = 600\text{mA}$	-	-	1.5	V
Base-Emitter Saturation Voltage <sup>1</sup>	$V_{BE(on)}$	$I_C = 6\text{A}, V_{CE} = 4\text{V}$	-	-	2	V
<b>SMALL SIGNAL CHARACTERISTICS<sup>2</sup></b>						
Transition Frequency <sup>3</sup>	$f_T$	$V_{CE} = 10\text{V}, I_C = 500\text{mA}, f_{TEST} = 1\text{MHz}$	3	-	-	MHZ
Small Signal Current Gain	$h_{fe}$	$V_{CE} = 10\text{V}, I_C = 500\text{mA}, f = 1\text{MHz}$	20	-	-	-

1. Pulsed duration = 300 ms, duty cycle  $\geq 1.5\%$
2. Not production testing in die form, characterized by chip design and package verification
3.  $f_T = |h_{fe}| \cdot f_{TEST}$

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