

# PNP Transistor Bare Die - TIP32C

Rev 1.1 10/01/24

#### Bipolar Medium Power Transistor in bare die form

Complement to NPN TIP31C

#### Features:

- Collector current up to 3A
- High switching speed
- Improved h<sub>FE</sub> linearity
- Solderable back metal
- High Reliability tested grades for Military + Space

## Ordering Information:

The following part suffixes apply:

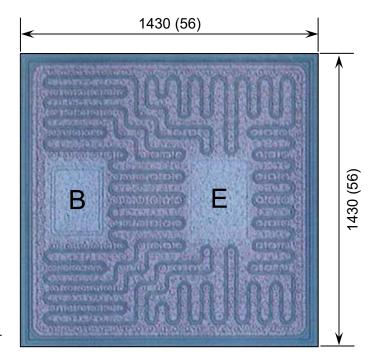
- No suffix Commercial grade die
- "H" Hi-rel grade die + MIL-STD-38534 Class H LAT
- "K" Hi-rel grade die + MIL-STD-38534 Class K LAT.

LAT = Lot acceptance Test.

For information on Hi-Rel LAT flows please see below.

www.siliconsupplies.com\bare-die-lot-qualification

## Die Dimensions in µm (mils)



**DIE BACK = COLLECTOR** 

### **Supply Formats:**

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape Specific request
- Unsawn Wafer Specific request
- With additional electrical selection Specific request
- Sawn as pairs or adjacent pair pick Specific request

### **Mechanical Specification**

Die Size (Excluding Saw Street)	1430 x 1430 56.30 x 56.30	µm mils	
Base Pad Size	310 x 430 12.20 x 16.93	µm mils	
Emitter Pad Size	310 x 430 12.20 x 16.93	µm mils	
Die Thickness	230 (±25) 9.06 (±1)	µm mils	
Top Metal Composition	Al		
Back Metal Composition	Ti/Ni/Ag		





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# Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V <sub>CBO</sub>	-100	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-100	V
Emitter-Base Voltage	V <sub>EBO</sub>	-5	V
Collector Current - Continuous	Ic	-3	Δ
Collector Current – Peak (t <sub>P</sub> < 5ms)	I <sub>CM</sub>	-5	7
Base Current	I <sub>B</sub>	-1	Α
Junction Temperature	TJ	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

#### Electrical Characteristics T<sub>A</sub> = 25°C unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Collector-Base Breakdown Voltage	V <sub>(BR)CBO</sub>	I <sub>E</sub> = 0	-100	-	-	V	
Collector-Emitter Sustaining Voltage <sup>1</sup>	V <sub>CEO(SUS)</sub>	I <sub>B</sub> = 0, I <sub>C</sub> = -30mA	-100	-	-	V	
Emitter-Base Breakdown Voltage	V <sub>(BR)EBO</sub>	I <sub>C</sub> = 0	-5	-	-	V	
Collector Cut-off Current	I <sub>CEO</sub>	V <sub>CE</sub> = -60V, I <sub>B</sub> = 0	-	-	-0.3	mA	
Emitter Cut-off Current	I <sub>EBO</sub>	V <sub>EB</sub> = -5V, I <sub>C</sub> = 0	-	-	-1	mA	
Collector Cut-off Current	I <sub>CES</sub>	V <sub>CE</sub> = -100V, V <sub>EB</sub> = 0	-	-	-0.2	mA	
ON CHARACTERISTICS							
Forward-Current Transfer Ratio <sup>1</sup>	h <sub>FE</sub>	I <sub>C</sub> = -1A, V <sub>CE</sub> = -4V	25	-	-	-	
		I <sub>C</sub> = -3.0A, V <sub>CE</sub> = -4V	10	-	50	-	
Collector-Emitter Saturation Voltage <sup>1</sup>	V <sub>CE(sat)</sub>	I <sub>C</sub> = -3A, I <sub>B</sub> = -375mA	-	-	-1.2	V	
Base-Emitter Saturation Voltage <sup>1</sup>	V <sub>BE(on)</sub>	$I_C = -3A, V_{CE} = -4V$	-	-	-1.8	V	
SMALL SIGNAL CHARACTERISTICS <sup>2</sup>							
Transition Frequency <sup>3</sup>	f⊤	$V_{CE}$ = -10V, $I_C$ = 500mA, $f_{TEST}$ = 1MHz	3	-	-	MHz	
Small Signal Current Gain	h <sub>fe</sub>	V <sub>CE</sub> = -10V, I <sub>C</sub> = 500mA, f = 1kHz	20	-	-	-	

<sup>1.</sup> Pulsed duration = 300 ms, duty cycle ≥1.5%

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<sup>2.</sup> Not production testing in die form, characterized by chip design and package verification

<sup>3.</sup>  $f_T = |h_{fe}| \circ f_{TEST}$