



NPN Transistor Bare Die - TIP31C

Rev 1.1
10/01/24

Bipolar Medium Power Transistor in bare die form
Complement to PNP TIP32C

Features:

- Collector current up to 3A
- High switching speed
- Improved h_{FE} linearity
- Solderable back metal
- High Reliability tested grades for Military + Space

Ordering Information:

The following part suffixes apply:

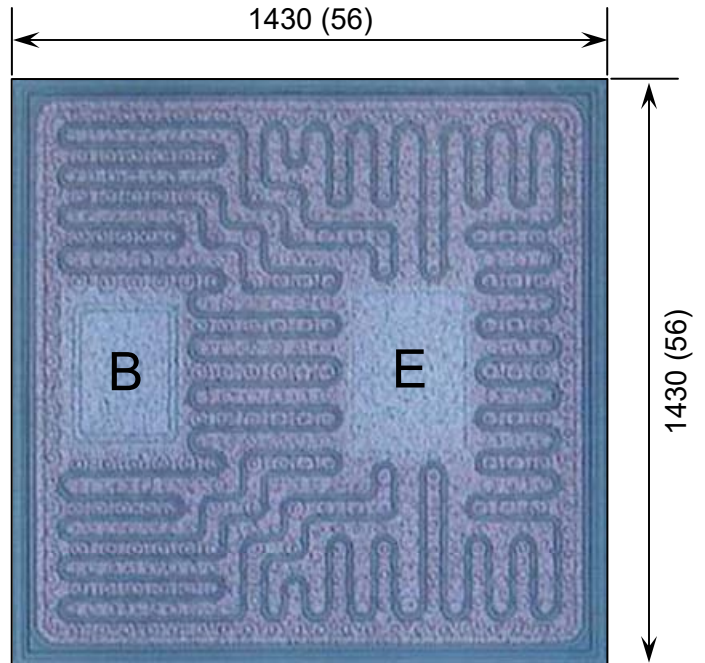
- No suffix - Commercial grade die
- "H" – Hi-rel grade die + MIL-STD-38534 Class H LAT
- "K" – Hi-rel grade die + MIL-STD-38534 Class K LAT.

LAT = Lot acceptance Test.

For information on Hi-Rel LAT flows please see below.

www.siliconsupplies.com/bare-die-lot-qualification

Die Dimensions in μm (mils)



DIE BACK = COLLECTOR

Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – Specific request
- Unsawn Wafer – Specific request
- With additional electrical selection – Specific request
- Sawn as pairs or adjacent pair pick – Specific request

Mechanical Specification

Die Size (Excluding Saw Street)	1430 x 1430 56.30 x 56.30	μm mils
Base Pad Size	310 x 430 12.20 x 16.93	μm mils
Emitter Pad Size	310 x 430 12.20 x 16.93	μm mils
Die Thickness	230 (± 25) 9.06 (± 1)	μm mils
Top Metal Composition	Al	
Back Metal Composition	Ti/Ni/Ag	





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Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V_{CBO}	100	V
Collector-Emitter Voltage	V_{CEO}	100	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current - Continuous	I_C	3	A
Collector Current – Peak ($t_P < 5\text{ms}$)	I_{CM}	5	
Base Current	I_B	1	A
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 150	$^\circ\text{C}$

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_E = 0$	100	-	-	V
Collector-Emitter Sustaining Voltage ¹	$V_{CEO(SUS)}$	$I_B = 0, I_C = 30\text{mA}$	100	-	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 0$	5	-	-	V
Collector Cut-off Current	I_{CEO}	$V_{CE} = 60\text{V}, I_B = 0$	-	-	0.3	mA
Emitter Cut-off Current	I_{EBO}	$V_{EB} = 5\text{V}, I_C = 0$	-	-	1	mA
Collector Cut-off Current	I_{CES}	$V_{CE} = 100\text{V}, V_{EB} = 0$	-	-	0.2	mA
ON CHARACTERISTICS						
Forward-Current Transfer Ratio ¹	h_{FE}	$I_C = 1\text{A}, V_{CE} = 4\text{V}$	25	-	-	-
		$I_C = 3.0\text{A}, V_{CE} = 4\text{V}$	10	-	50	-
Collector-Emitter Saturation Voltage ¹	$V_{CE(sat)}$	$I_C = 3\text{A}, I_B = 375\text{mA}$	-	-	1.2	V
Base-Emitter Saturation Voltage ¹	$V_{BE(on)}$	$I_C = 3\text{A}, V_{CE} = 4\text{V}$	-	-	1.8	V
SMALL SIGNAL CHARACTERISTICS²						
Transition Frequency ³	f_T	$V_{CE} = 10\text{V}, I_C = 500\text{mA}, f_{TEST} = 1\text{MHz}$	3	-	-	MHz
Small Signal Current Gain	h_{fe}	$V_{CE} = 10\text{V}, I_C = 500\text{mA}, f = 1\text{kHz}$	20	-	-	-

1. Pulsed duration = 300 ms, duty cycle $\geq 1.5\%$
2. Not production testing in die form, characterized by chip design and package verification
3. $f_T = |h_{fe}| \cdot f_{TEST}$

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