



# PNP Transistor Bare Die – TIP117

Rev 1.0  
22/08/23

**Bipolar Darlington Power Transistor in bare die form**  
Complement to NPN TIP112

## Features:

- Collector current up to 2A
- Low  $V_{CE(sat)}$
- Very high  $h_{FE}$
- Solderable back metal
- High Reliability tested grades for Military + Space

## Ordering Information:

The following part suffixes apply:

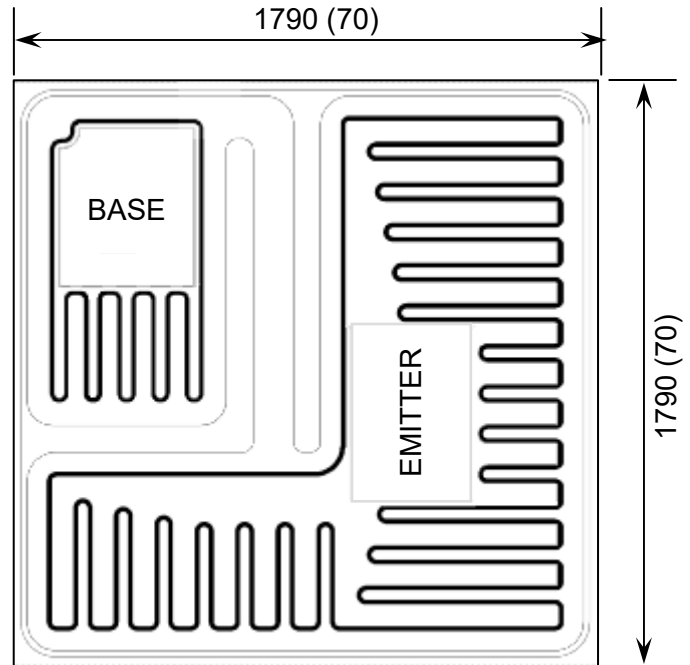
- No suffix - Commercial grade die
- “H” – Hi-rel grade die + MIL-STD-38534 Class H LAT
- “K” – Hi-rel grade die + MIL-STD-38534 Class K LAT.

LAT = Lot acceptance Test.

For information on Hi-Rel LAT flows please see below.

[www.siliconsupplies.com/bare-die-lot-qualification](http://www.siliconsupplies.com/bare-die-lot-qualification)

## Die Dimensions in $\mu\text{m}$ (mils)



**DIE BACK = COLLECTOR**

## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – Specific request
- Unsawn Wafer – Specific request
- With additional electrical selection – Specific request
- Sawn as pairs or adjacent pair pick – Specific request

## Mechanical Specification

Die Size (Excluding Saw Street)	1790 x 1790 70.47 x 70.47	$\mu\text{m}$ mils
Emitter Pad Size	374 x 524 14.72 x 20.63	$\mu\text{m}$ mils
Base Pad Size	408 x 578 16.06 x 22.76	$\mu\text{m}$ mils
Die Thickness	260 ( $\pm 25$ ) 10.2 ( $\pm 1$ )	$\mu\text{m}$ mils
Top Metal Composition	Al	
Back Metal Composition	Ti/Ni/Ag	





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## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	$V_{CBO}$	100	V
Collector-Emitter Voltage	$V_{CEO}$	100	V
Emitter-Base Voltage	$V_{EBO}$	5	V
Collector Current - Continuous	$I_C$	2	A
Collector Current – Peak ( $t_P < 5\text{ms}$ )	$I_{CM}$	4	
Base Current	$I_B$	50	mA
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$

## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Collector-Emitter Sustaining Voltage <sup>1</sup>	$V_{CEO(SUS)}$	$I_B = 0, I_C = 30\text{mA}$	100	-	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 0$	5	-	-	V
Collector Cut-off Current	$I_{CEO}$	$V_{CE} = 50\text{V}, I_B = 0$	-	-	2	mA
Emitter Cut-off Current	$I_{EBO}$	$V_{EB} = 5\text{V}, I_C = 0$	-	-	2	mA
Collector Cut-off Current	$I_{CBO}$	$V_{CB} = 100\text{V}, I_E = 0$	-	-	1	mA
<b>ON CHARACTERISTICS</b>						
Forward-Current Transfer Ratio <sup>1</sup>	$h_{FE}$	$I_C = 1\text{A}, V_{CE} = 4\text{V}$	1000	-	-	-
		$I_C = 2\text{A}, V_{CE} = 4\text{V}$	500	-	-	-
Collector-Emitter Saturation Voltage <sup>1</sup>	$V_{CE(sat)}$	$I_C = 2\text{A}, I_B = 8\text{mA}$	-	-	2.5	V
Base-Emitter Saturation Voltage <sup>1</sup>	$V_{BE(on)}$	$I_C = 2\text{A}, V_{CE} = 4\text{V}$	-	-	2.8	V
<b>SMALL SIGNAL CHARACTERISTICS<sup>2</sup></b>						
Small-Signal Current Gain	$h_{fe}$	$V_{CE} = 10\text{V}, I_C = 0.75\text{A}, f = 1\text{MHz}$	25	-	-	-
Output Capacitance	$C_{ob}$	$V_{CB} = 10\text{V}, I_E = 0, f = 0.1\text{MHz}$	-	-	150	pF

1. Pulsed duration = 300  $\mu\text{s}$ , duty cycle  $\leq 2.0\%$

2. Not production testing in die form, characterized by chip design and package verification

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