Quad Channel Digital Isolator – SiS8017

High-Speed, EMC Ruggedized CMOS / LVCMOS Digital Isolator in bare die form

Rev 1.0
10/03/25

Description

SiS8017 quad channel digital isolator consists of two forward and two reverse-direction isolated channels. Each channel has a logic input & output buffer separated by a double-capacitive silicon dioxide (SiO_2) insulation barrier to provide up to 5000 V_{RMS} isolation rating[2] per UL 1577.

Enable pins are used to place their respective outputs in high impedance for multi-master driving applications and to reduce power consumption. If the input power or signal is lost, outputs default to high impedance state.

Used with isolated power supplies, SiS8017 prevents noise current on data buses, such as RS-485, RS-232 or CAN. Ancillary circuits are also prevented from entering the local ground to disrupt or damage sensitive circuitry. Via innovative chip design, high electromagnetic immunity, low emissions and low power consumption enable system-level improvement in ESD, EFT, surge and emission compliance.

Features:

- CMOS or LVCMOS I/O capability
- Up to 100 Mbps data rate
- Robust isolation barrier:
  - Up to 5000 V_{RMS} isolation rating[2]
  - Up to 12.8 kV surge capability
  - ±95 kV/µs typical CMTI
- Wide supply range: 2.25V to 5.5V
- 2.25V to 5.5V level translation
- Wide temperature range: -55°C to 125°C
- Low power consumption:
  - typical 1.5mA per channel at 1 Mbps
- Low propagation delay: 19ns typical (5V supply)
- Robust electromagnetic compatibility (EMC)

Ordering Information

The following part suffixes apply:

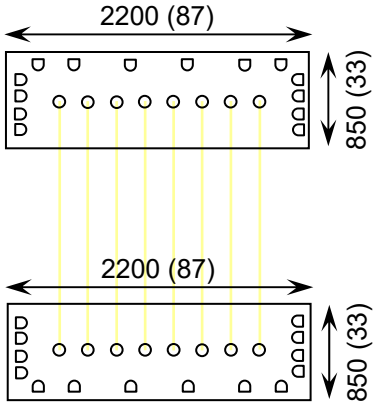
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into SOIC-16 Package – On request

Mechanical Specification

Die Size (Un-sawn)	2200 x 850 87 x 33	µm mils
Minimum Bond Pad Size	57 x 57 2.24 x 2.24	µm mils
Die Thickness	280 (±20) 11 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 4µm	
Back Metal Composition	N/A – Bare Si	

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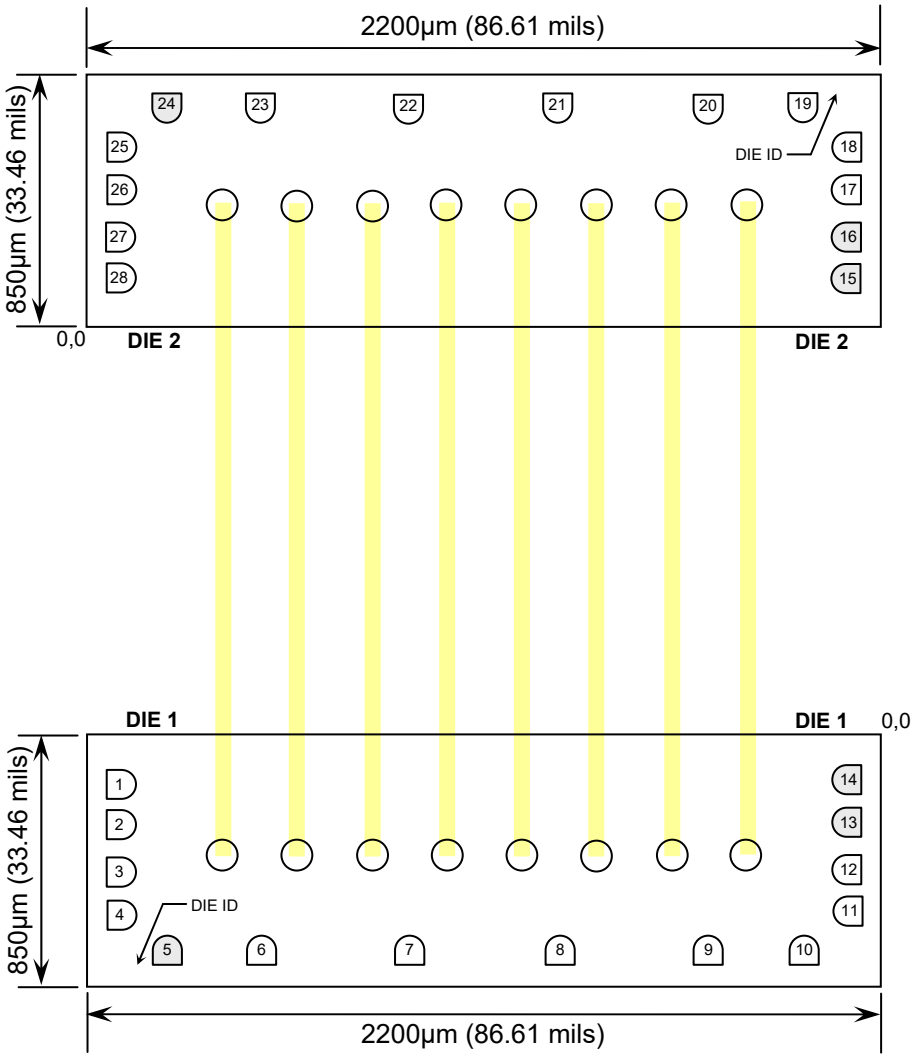
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
DIE 1			
1	VCC1	-2123	-115
2	VCC1	-2123	-210
3	GND1	-2123	-580
4	GND1	-2123	-675
5	NO CONNECT	-1955	-769
6	IN_A	-1686	-769
7	IN_B	-1276	-769
8	OUT_C	-866	-769
9	OUT_D	-456	-769
10	EN_1	-188	-769
11	GND1	-20	-675
12	GND1	-20	-580
13	NO CONNECT	-20	-210
14	NO CONNECT	-20	-115
DIE 2			
15	NO CONNECT	2123	115
16	NO CONNECT	2123	210
17	GND2	2123	580
18	GND2	2123	675
19	EN2	1955	769
20	IN_D	1686	769
21	IN_C	1276	769
22	OUT_B	866	769
23	OUT_A	456	769
24	NO CONNECT	188	769
25	GND2	20	675
26	GND2	20	580
27	VCC2	20	210
28	VCC2	20	115
ISOLATE CHIP BACKSIDES (DIE 1 & DIE 2)			

SUGGESTED MATERIALS	
WIREBOND	Al 17.5µm (0.7 Mils)
DIE ATTACH	NON-CONDUCTIVE EPOXY
MOLD COMPOUND	CEL-9240HF10XZ-M1 (FULLY ENCAPSULATED ASSEMBLIES)
DAM & FILL GLOB COATING	DELO® MONOPOX GE6585 – DAM DELO® MONOPOX GE6525 - FILL (DIE-TO-DIE WIRE BONDS IN CAVITY ASSEMBLIES)

MINIMUM PAD OPENING SIZE	
PERIPHERAL	57 x 57µm (2.24 x 2.24 Mils)
DIE-TO-DIE	Ø 90 µm (Ø 3.54 Mils)

***** PLEASE NOTE *****

The assembly materials suggested are provided on an example basis only and are not a guarantee of conditions or characteristics. The IC's operating characteristics & maximum isolation voltages are affected by the length, material + thickness of die-to-die bond wires and also coating material & it's distribution. Users are advised to verify that performance, material section & assembly method is suitable for the end application usage.

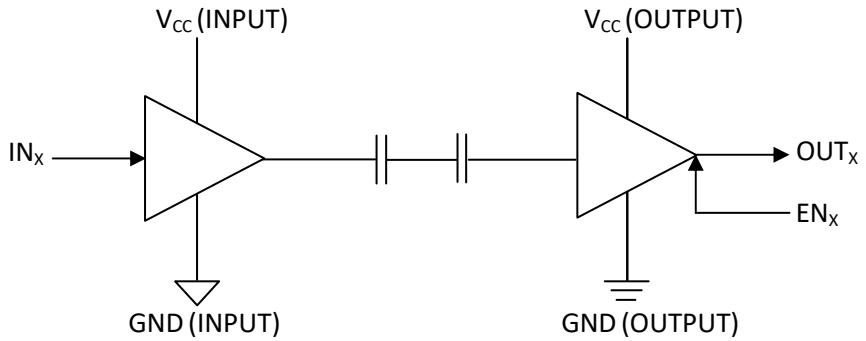
Pad Descriptions

PAD	SYMBOL	DESCRIPTION
1 - 2	VCC1	Power supply – DIE 1
3 - 4	GND1	Ground connection for VCC1
5	NO CONNECT	Not connected
6	IN_A	Input, Channel A
7	IN_B	Input, Channel B
8	OUT_C	Output, Channel C
9	OUT_D	Output, Channel D
10	EN1	Output enable 1 Outputs on DIE 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
11 - 12	GND1	Ground connection for VCC1
13 - 16	NO CONNECT	Not connected
17 -18	GND2	Ground connection for VCC2
19	EN2	Output enable 2 Outputs on DIE 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
20	IN_D	Input, Channel D
21	IN_C	Input, Channel C
22	OUT_B	Output, Channel B
23	OUT_A	Output, Channel A
24	NO CONNECT	Not connected
25 - 26	GND2	Ground connection for VCC2
27 - 28	VCC2	Power supply – DIE 2

Functional Operation

Using an ON-OFF keying (OOK) modulation protocol, digital data is transmitted across a SiO_2 based isolation barrier. The transmitting die sends a high-frequency carrier across the isolation barrier via wire-bond to represent one digital state whereas the other digital state is represented by no signal. The receiving die demodulates the signal after advanced signal conditioning to produce an isolated output through a buffer stage. If the enable on either die is pulled low, then the output goes to high impedance. CMTI performance is maximised and radiated emissions are minimised via a combination of the high frequency carrier circuitry plus input/output buffer switching.

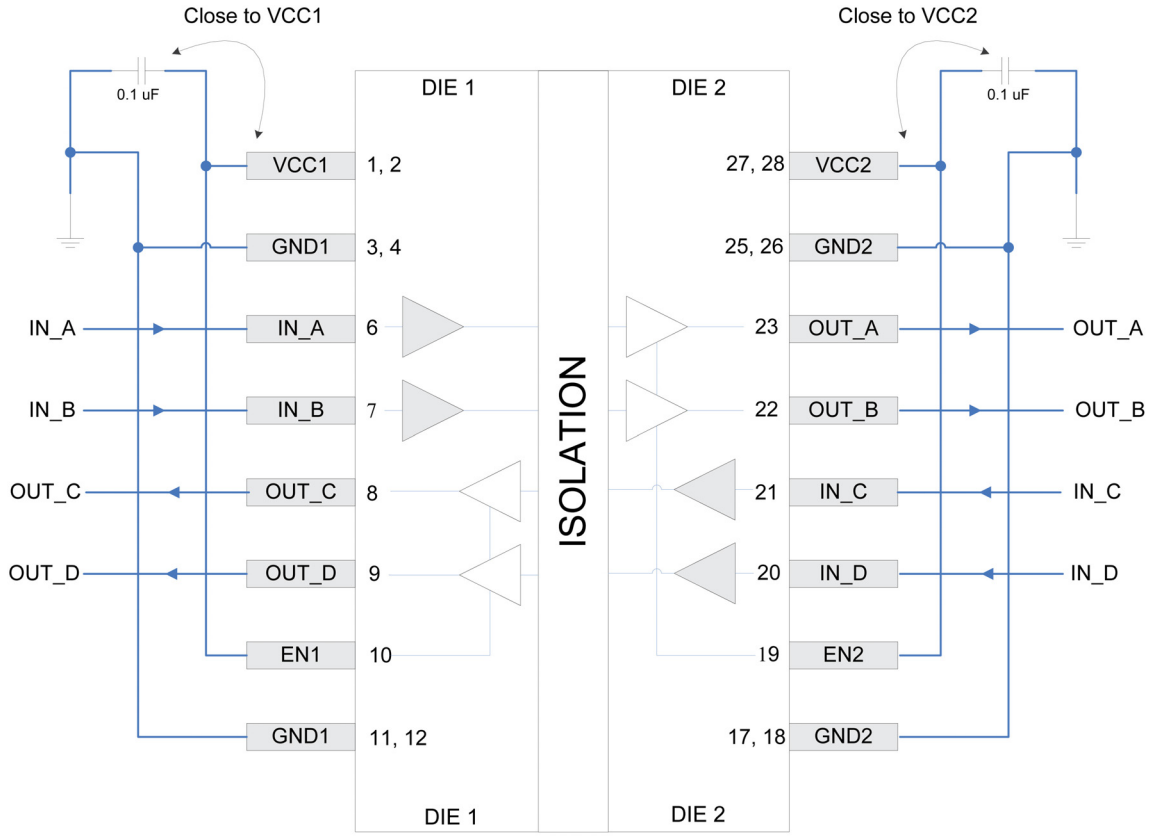
Simplified Block Diagram



Applications

- Motor Control
- Medical Equipment
- Industrial Automation
- Hi-Rel Sensors
- Solar Inverters
- 2.25V to 5.5V level translation
- Isolated MCP/MCM integrations

Connection Schematic

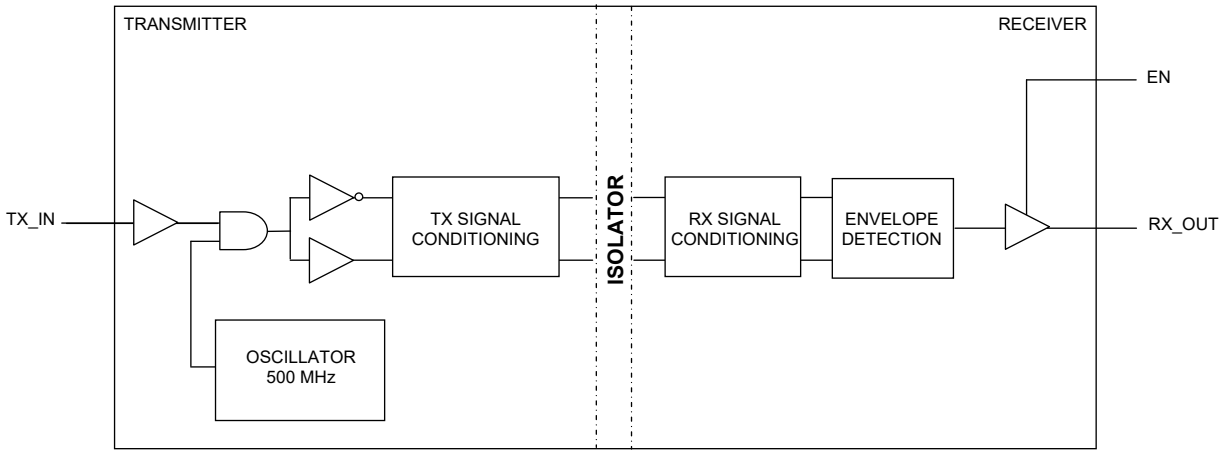


* To help ensure reliable operation at data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at the input and output supply pins (VCC1 and VCC2). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in the application, isolated power can be generated for the secondary-side with the help of a transformer.

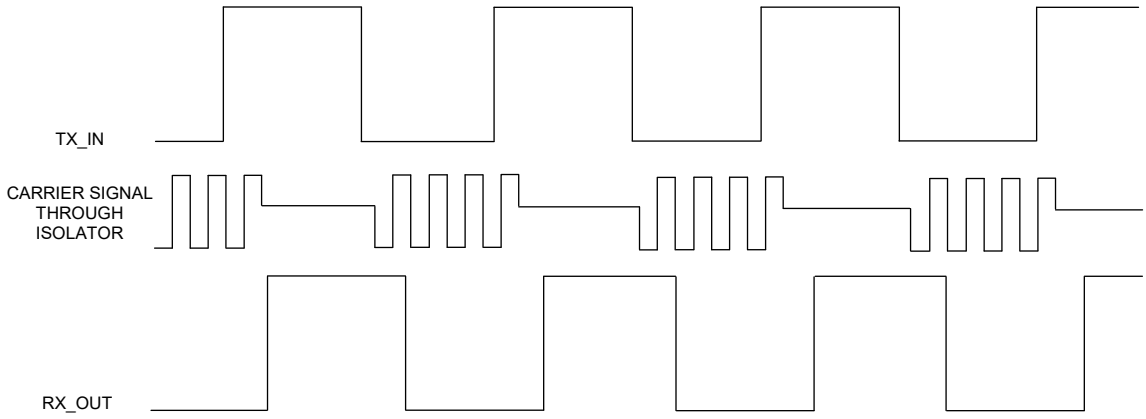
Truth Table

VCCI	VCCO	INPUT	OUTPUT ENABLE	OUTPUT	COMMENTS
POWERED UP	POWERED UP	HIGH	HIGH OR OPEN	HIGH	NORMAL OPERATION
POWERED UP	POWERED UP	LOW	HIGH OR OPEN	LOW	NORMAL OPERATION
POWERED UP	POWERED UP	OPEN	HIGH OR OPEN	HIGH	DEFAULT MODE
IRRELEVANT	POWERED UP	IRRELEVANT	LOW	HIGH IMPEDANCE	DEFAULT MODE
POWERED DOWN	POWERED UP	IRRELEVANT	HIGH OR OPEN	HIGH	DEFAULT MODE
IRRELEVANT	POWERED DOWN	IRRELEVANT	IRRELEVANT	UNDETERMINED	-

Signal Chain



On-Off Keying (OOK) Modulation Scheme



Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE		UNIT
Supply Voltage Range	V_{CC1}, V_{CC2}	-0.5 to +6		V
Voltage at IN_X, OUT_X, EN_X	V	-0.5 to V_{CCX} +0.5		V
Output Current	I_O	±15		mA
Storage Temperature	T_{STG}	-65 to +150		°C
Operating Junction Temperature	T_J	-40 to 150		°C
Isolation Voltage[2]	V_{ISO}	5		kV
Electrostatic Discharge (HBM)[3]	V_{ESD}	8		kV
Power Dissipation Total[2]	P_D	V_{CC1} = V_{CC2} = 5.5V,T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	200	mW
Power Dissipation Die 1[2]	P_{D1}		100	mW
Power Dissipation Die 2[2]	P_{D2}		100	mW
Thermal Resistance,Junction-to-ambient[2]	$R_{\theta JA}$	85		°C/W

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic SOIC-16 package, results in die form are dependent on die attach, substrate and assembly methods. **3.** Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins

Recommended Operating Conditions, V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Supply Voltage	V_{CC1}, V_{CC2}	-	2.25	-	5.5	V
UVLO threshold	$V_{CC(UVLO+)}$	Supply Voltage rising	-	2	2.25	V
	$V_{CC(UVLO+)}$	Supply Voltage falling	1.7	1.8	-	V
Supply Voltage UVLO hysteresis	$V_{HYS(UVLO)}$	-	100	200	-	mV
High-Level Output Current	I_{OH}	V_{CCO} = 5V	-4	-	-	mA
		V_{CCO} = 3.3V	-2	-	-	
		V_{CCO} = 2.5V	-1	-	-	
Low-Level Output Current	I_{OL}	V_{CCO} = 5V	-	-	4	mA
		V_{CCO} = 3.3V	-	-	2	
		V_{CCO} = 2.5V	-	-	1	
High-Level Input Voltage	V_{IH}	-	0.7 x V_{CCI}	-	V_{CCI}	V
Low-Level Input Voltage	V_{IL}	-	0	-	0.3 x V_{CCI}	V
Data Rate[4]	DR	-	0	-	100	Mbps
Ambient Temperature	T_A	-	-55	25	125	°C

4. 100 Mbps is the maximum specified data rate, equivalent generator: pulse PRR = 50 MHz, 50% duty cycle.

Safety Limiting Values[2, 5]

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Safety input, output, or supply current	I_S	$R_{\theta JA}$ = 85°C/W, T_J = 150°C, T_A = 25°C	V_I = 5V	-	-	280	mA
			V_I = 3.3V	-	-	425	
			V_I = 2.5V	-	-	560	
Safety input, output, or total power[6]	P_S	$R_{\theta JA}$ = 85 °C/W, T_J = 150°C, T_A = 25°C		-	-	1400	mW
Maximum safety Temperature[7]	T_S	-		-	-	150	°C

5. Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures. **6.** Maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. **7.** Power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

DC Characteristics 5V, V_{CC1} = V_{CC2} = 5V, V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
High-Level Output Voltage	V_{OH}	I_{OH} = -4mA, Figure 1		V_{CCO} -0.4	V_{CCO} -0.2	-	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 4mA, Figure 1		-	0.2	0.4	V
Rising Input Voltage Threshold	$V_{IT+(IN)}$	-		-	0.6 x V_{CCI}	0.7 x V_{CCI}	V
Falling Input Voltage Threshold	$V_{IT-(IN)}$	-		0.3 x V_{CCI}	0.4 x V_{CCI}	-	V
Input Voltage Threshold Hysteresis	$V_{I(HYS)}$	-		0.1 x V_{CCI}	0.2 x V_{CCI}	-	V
High-Level Input Current	I_{IH}	V_{IH} = V_{CCI} at INx or ENx		-	-	10	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V at INx or ENx		-10	-	-	µA
Common-Mode Transient Immunity	CMTI	V_I = V_{CCI} or 0V, V_{CM} = 1200V, Figure 4		tbd	tbd	-	kV/µs
Supply Current - Disable	I_{CC1}, I_{CC2}	EN1 = EN2 = 0V; V_I = V_{CCI}		-	0.9	2.0	mA
		EN1 = EN2 = 0V; V_I = 0V		-	3.0	4.6	mA
Supply Current - DC Signal	I_{CC1}, I_{CC2}	EN1 = EN2 = V_{CCI}; V_I = V_{CCI}		-	1.7	3.5	mA
		EN1 = EN2 = V_{CCI}; V_I = 0V		-	4.0	6.0	mA
Supply Current - AC Signal	I_{CC1}, I_{CC2}	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	-	3.0	4.9	mA
			10 Mbps	-	4.0	6.0	mA
			100 Mbps	-	13.4	18.3	mA

DC Characteristics 3.3V, V_{CC1} = V_{CC2} = 3.3V, V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA, Figure 1		V_{CCO} -0.3	V_{CCO} -0.1	-	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 2mA, Figure 1		-	0.1	0.3	V
Rising Input Voltage Threshold	$V_{IT+(IN)}$	-		-	0.6 x V_{CCI}	0.7 x V_{CCI}	V
Falling Input Voltage Threshold	$V_{IT-(IN)}$	-		0.3 x V_{CCI}	0.4 x V_{CCI}	-	V
Input Voltage Threshold Hysteresis	$V_{I(HYS)}$	-		0.1 x V_{CCI}	0.2 x V_{CCI}	-	V
High-Level Input Current	I_{IH}	V_{IH} = V_{CCI} at INx or ENx		-	-	10	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V at INx or ENx		-10	-	-	µA
Common-Mode Transient Immunity	CMTI	V_I = V_{CCI} or 0V, V_{CM} = 1200V , Figure 4		tbd	tbd	-	kV/µs
Supply Current - Disable	I_{CC1}, I_{CC2}	EN1 = EN2 = V_{CCI}; V_I = V_{CCI}		-	0.9	2.0	mA
		EN1 = EN2 = V_{CCI}; V_I = 0V		-	3.0	4.6	mA
Supply Current - DC Signal	I_{CC1}, I_{CC2}	EN1 = EN2 = V_{CCI}; V_I = V_{CCI}		-	1.7	3.4	mA
		EN1 = EN2 = V_{CCI}; V_I = 0V		-	4.0	5.9	mA
Supply Current - AC Signal	I_{CC1}, I_{CC2}	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	-	3.0	4.8	mA
			10 Mbps	-	3.6	5.6	mA
			100 Mbps	-	10.3	14.4	mA

DC Characteristics 2.5V, V_{CC1} = V_{CC2} = 2.5V, V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
High-Level Output Voltage	V_{OH}	I_{OH} = -1mA, Figure 1	V_{CCO} -0.2	V_{CCO} -0.05	-	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1mA, Figure 1	-	0.05	0.2	V
Rising Input Voltage Threshold	$V_{IT+(IN)}$	-	-	0.6 x V_{CCI}	0.7 x V_{CCI}	V
Falling Input Voltage Threshold	$V_{IT-(IN)}$	-	0.3 x V_{CCI}	0.4 x V_{CCI}	-	V
Input Voltage Threshold Hysteresis	$V_{I(HYS)}$	-	0.1 x V_{CCI}	0.2 x V_{CCI}	-	V
High-Level Input Current	I_{IH}	V_{IH} = V_{CCI} at INx or ENx	-	-	10	µA
Low-Level Input Current	I_{IL}	V_{IL} = 0V at INx or ENx	-10	-	-	µA

DC Characteristics 2.5V Cont., V_{CC1} = V_{CC2} = 2.5V, V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Common-Mode Transient Immunity	CMTI	V_I = V_{CCI} or 0V, V_{CM} = 1200V , Figure 4		tbd	tbd	-	kV/µs
Supply Current - Disable	I_{CC1}, I_{CC2}	EN1 = EN2 = 0V; V_I = V_{CCI}		-	0.9	1.9	mA
		EN1 = EN2 = 0V; V_I = 0V		-	3.0	4.6	mA
Supply Current - DC Signal	I_{CC1}, I_{CC2}	EN1 = EN2 = V_{CCI}; V_I = V_{CCI}		-	1.7	3.4	mA
		EN1 = EN2 = V_{CCI}; VI = 0 V		-	4.0	5.9	mA
Supply Current - AC Signal	I_{CC1}, I_{CC2}	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	-	2.9	4.7	mA
			10 Mbps	-	3.4	5.4	mA
			100 Mbps	-	8.3	11.9	mA

Switching Characteristics 5V, V_{CC1} = V_{CC2} = 5V

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Propagation Delay Time	t_{PHL}, t_{PLH}	See Figure 1	-	19	24	ns
Pulse Width Distortion[8]	PWD $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 1	-	2	7	ns
Channel-to-Channel output skew time[9]	$t_{sk(o)}$	Same-direction channels	-	-	4	ns
Part-to-Part skew time[10]	$t_{sk(pp)}$	-	-	-	4.4	ns
Output Signal Rise Time	t_r	See Figure 1	-	1.5	2.4	ns
Output Signal Fall Time	t_f	See Figure 1	-	1.5	2.4	ns
Disable Propagation Delay, high-to-high impedance output	t_{PHZ}	See Figure 2	-	9	20	ns
Disable Propagation Delay, low-to-high impedance output	t_{PLZ}	See Figure 2	-	9	20	ns
Enable Propagation Delay,high impedance-to-high output	t_{PZH}	See Figure 2	-	7	20	ns
Enable Propagation Delay,high impedance-to-low output	t_{PZL}	See Figure 2	-	3	8.5	ns
Default output delay time from input power loss	t_{DO}	Measured from the time V_{CC} goes below 1.7 V. See Figure 3	-	0.1	0.3	µs

Switching Characteristics 3.3V, $V_{CC1} = V_{CC2} = 3.3V$

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay Time	t_{PHL}, t_{PLH}	See Figure 1	-	21	27	ns
Pulse Width Distortion[8]	PWD $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 1	-	3	7	ns
Channel-to-Channel output skew time[9]	$t_{sk(o)}$	Same-direction channels	-	-	4.1	ns
Part-to-Part skew time[10]	$t_{sk(pp)}$	-	-	-	4.5	ns
Output Signal Rise Time	t_r	See Figure 1	-	1.7	3.5	ns
Output Signal Fall Time	t_f	See Figure 1	-	2.1	3.5	ns
Disable Propagation Delay, high-to-high impedance output	t_{PHZ}	See Figure 2	-	17	30	ns
Disable Propagation Delay, low-to-high impedance output	t_{PLZ}	See Figure 2	-	17	30	ns
Enable Propagation Delay,high impedance-to-high output	t_{PZH}	See Figure 2	-	17	30	ns
Enable Propagation Delay,high impedance-to-low output	t_{PZL}	See Figure 2	-	3.2	8.5	ns
Default output delay time from input power loss	t_{DO}	Measured from the time V_{CC} goes below 1.7 V. See Figure 3	-	0.1	0.3	µs

Switching Characteristics 2.5V, $V_{CC1} = V_{CC2} = 2.5V$

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay Time	t_{PHL}, t_{PLH}	See Figure 1	-	24	29	ns
Pulse Width Distortion[8]	PWD $\lvert t_{PHL} - t_{PLH} \rvert$	See Figure 1	-	4	8	ns
Channel-to-Channel output skew time[9]	$t_{sk(o)}$	Same-direction channels	-	-	4.1	ns
Part-to-Part skew time[10]	$t_{sk(pp)}$	-	-	-	4.6	ns

Switching Characteristics Continued 2.5V, $V_{CC1} = V_{CC2} = 2.5V$

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Output Signal Rise Time	t_r	See Figure 1	-	3.5	4.5	ns
Output Signal Fall Time	t_f	See Figure 1	-	3.5	4.5	ns
Disable Propagation Delay, high-to-high impedance output	t_{PHZ}	See Figure 2	-	22	40	ns
Disable Propagation Delay, low-to-high impedance output	t_{PLZ}	See Figure 2	-	22	40	ns
Enable Propagation Delay,high impedance-to-high output	t_{PZH}	See Figure 2	-	18	40	ns
Enable Propagation Delay,high impedance-to-low output	t_{PZL}	See Figure 2	-	3.3	8.5	ns
Default output delay time from input power loss	t_{DO}	Measured from the time V_{CC} goes below 1.7 V. See Figure 3	-	0.1	0.3	µs

8. Also known as Pulse Skew. **9.** $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads. **10.** $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices.

Test & Measurement Circuits

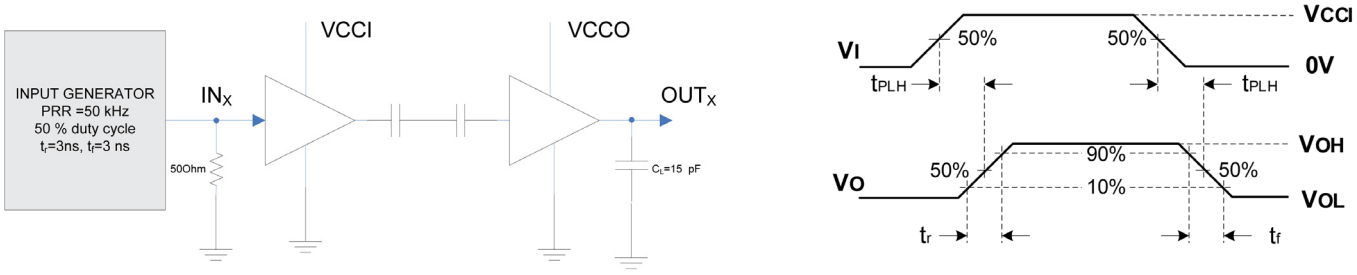


Figure 1 – Switching Characteristics Test Circuit and Voltage Waveforms

Test & Measurement Circuits continued

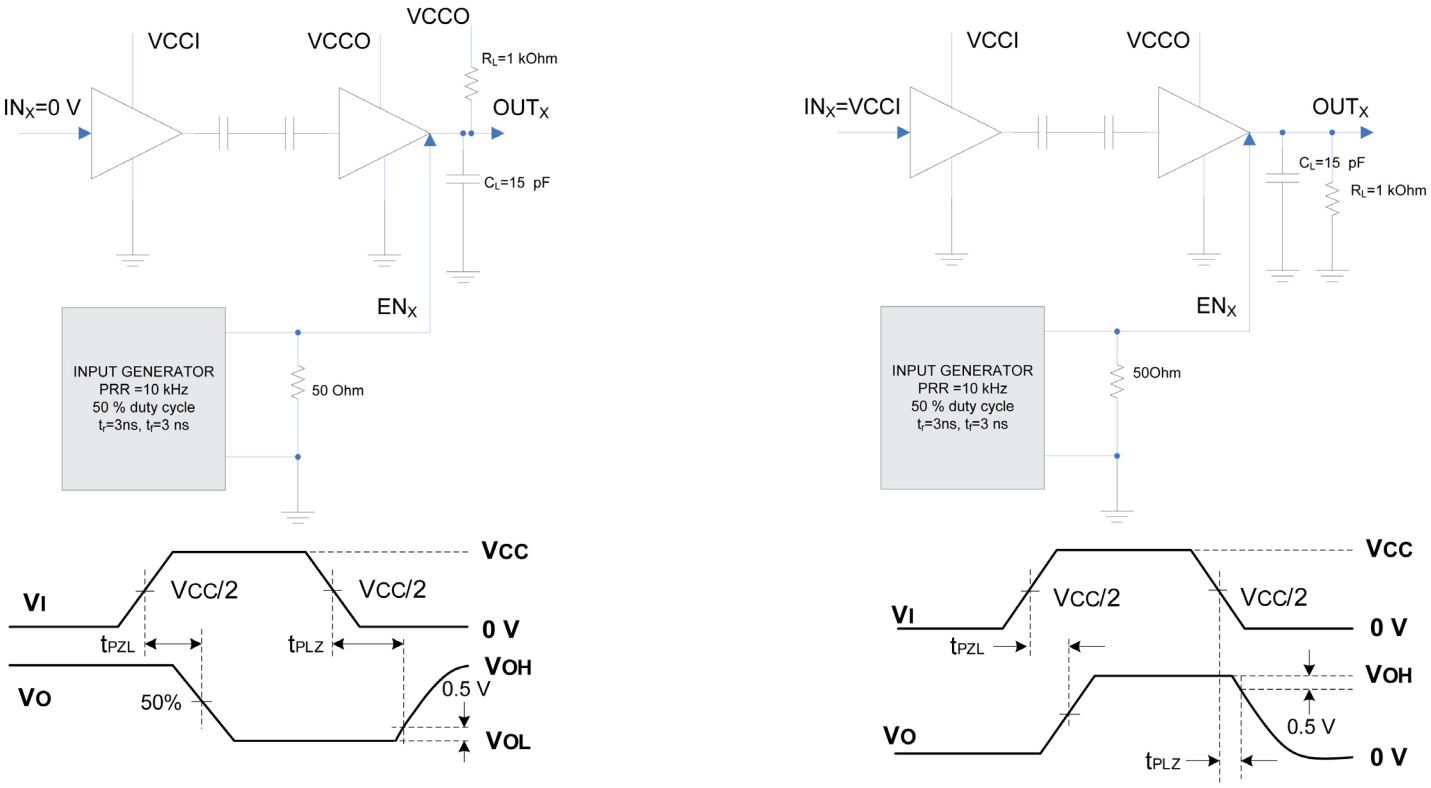


Figure 2 – Enable/Disable Propagation Delay Time Test Circuit and Waveform

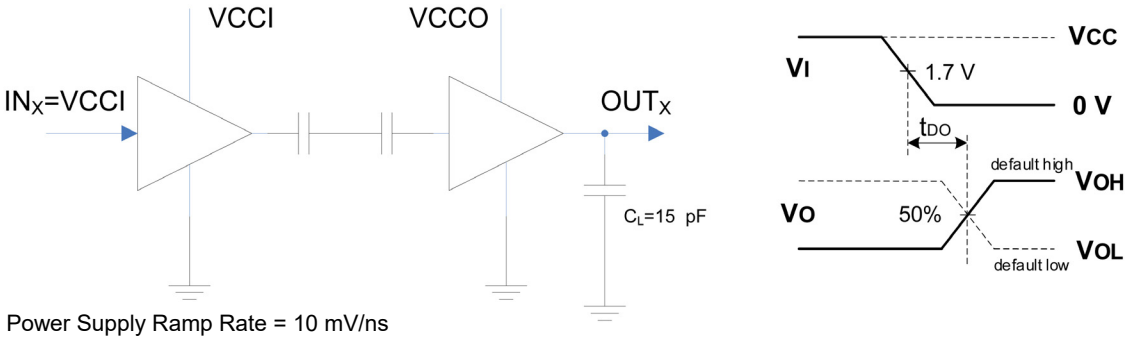
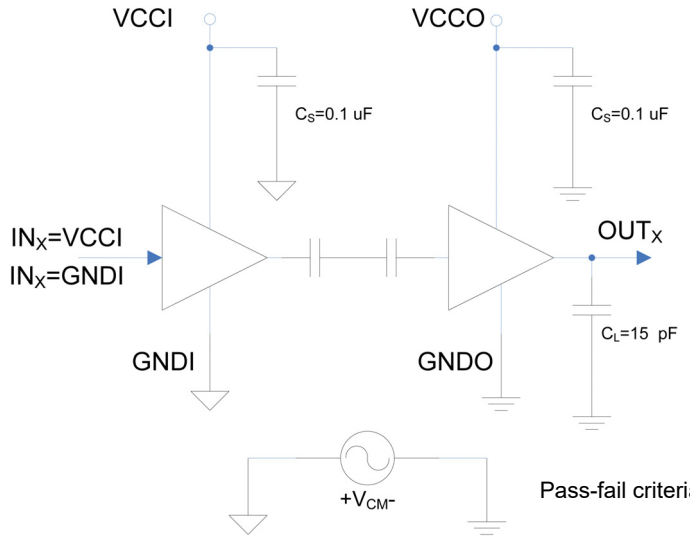


Figure 3 – Default Output Delay Time Test Circuit and Voltage Waveforms

Test & Measurement Circuits continued



Pass-fail criteria: the output must remain stable.

Figure 4 – Common-Mode Transient Immunity Test Circuit

Input / Output Schematics