Small Signal MOSFET – SiS60VP02

Rev 1.0
17/06/26

P-Channel Enhancement Mode Field Effect Transistor in bare die form

Features:

- High density cell design for low $R_{DS(ON)}$
- Low Threshold Voltage
- ESD protected Gate
- Suited for High-Speed Switching & Analog Switching
- High Reliability tested grades for Military + Space

Ordering Information:

The following part suffixes apply:

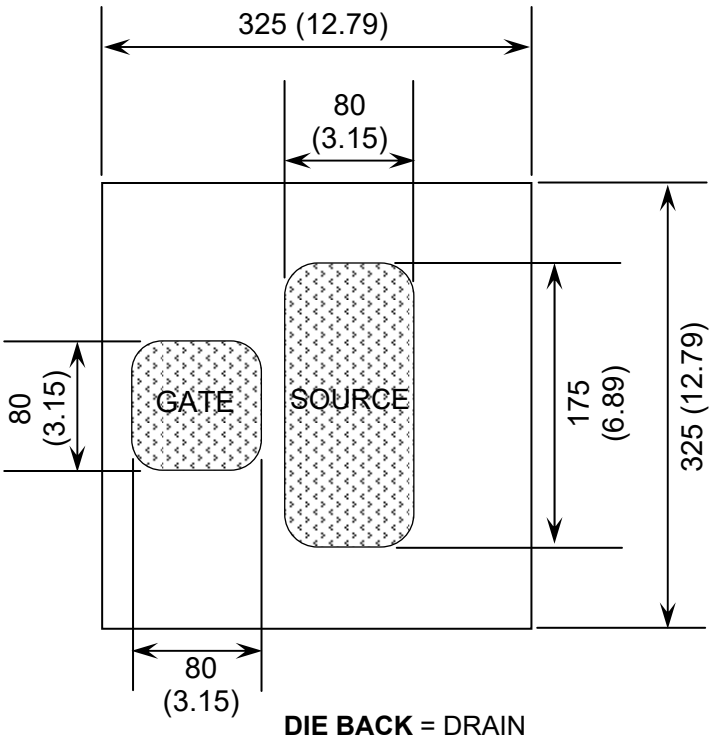
- No suffix - MIL-STD-750 /2072 Visual Inspection
- "**H**" - MIL-STD-750 /2072 Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-750 /2072 Visual Inspection
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



DIE BACK = DRAIN

Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- With additional electrical selection – On request
- Sawn as pairs or adjacent pair pick – On request
- Assembled in package – On request

Mechanical Specification

Die Size (Including Saw Street)	325 x 325 12.79 x 12.79	µm mils
Gate Pad Size	80 x 80 3.15 x 3.15	µm mils
Source Pad Size	80 x 175 3.15 x 6.89	µm mils
Die Thickness	152 (±10) 6 (±0.39)	µm mils
Top Metal Composition	Al/Cu	
Back Metal Composition	Ti/Ni/Ag/Sn	

Absolute Maximum Ratings[1] T_J = 25°C unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Drain-to-Source Voltage	V_{DSS}	-60	V
Gate-Source Voltage - Continuous	V_{GSS}	±20	V
Maximum Drain Current - Continuous	I_D	-210	mA
Maximum Drain Current - Pulsed		-530	
Maximum Power Dissipation Derated above 25°C[2]	P_D	360	mW
THERMAL CHARACTERISTICS			
Junction & Storage Temperature	T_J, T_{stg}	-55 to 150	°C
Thermal Resistance, Junction to Ambient[2, 3]	$R_{\theta JA}$	350	°C/W

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Die level performance dependent on assembly method & substrate choice 3. SOT-23 package mounted on 1in^2 FR-4 board with 1oz pin.

Electrical Characteristics T_J = 25°C unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48V, V_{GS} = 0	-	-	-1	µA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±10	
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250µA	-1.0	-1.6	-2.5	V
Static Drain-Source On-Resistance[4]	$R_{DS(on)}$	V_{GS} = -10V, I_D = -100mA	-	4.0	6.0	Ω
		V_{GS} = -4.5V, I_D = -100mA	-	4.5	7.0	
Forward Transfer Admittance	|Yfs|	V_{DS} = -5V, I_D = -100mA	-	4.4	-	S
DYNAMIC CHARACTERISTICS[5]						
Input Capacitance	C_{iss}	V_{DS} = -30V, V_{GS} = 0V, f = 1MHz	-	30	-	pF
Output Capacitance	C_{oss}		-	12	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = -10V,V_{DS}= -30V, I_D = -1A, R_{GEN} = 6Ω	-	18.4	-	ns
Rise Time	t_r		-	15.2	-	
Turn-Off Time	$t_{d(off)}$		-	113	-	
Fall Time	t_f		-	41	-	
Total Gate Charge	Q_g	V_{GS} = -4.5V,V_{DS} = -30V, I_D = -0.37A	-	0.47	-	nC
		V_{GS}= -10V,V_{DS}= -30V, I_D= -0.37A	-	0.84	-	
Gate-Source Charge	Q_{gs}	V_{GS}= -10V,V_{DS}= -30V, I_D= -0.37A	-	0.19	-	
Gate-Drain Charge	Q_{gd}		-	0.21	-	
SOURCE-DRAIN BODY DIODE CHARACTERISTICS						
Diode Forward Voltage[4]	V_F	I_F = -0.1A, V_{GS} = 0V	-	-0.8	-1.1	V
Reverse Recovery Time	t_{rr}	I_F= -0.18A, V_R = -30V, dI_F/dt = 100A/µs	-	10	-	ns
Reverse Recovery Charge	Q_{rr}		-	5	-	nC

4. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%. **5.** Not production tested in die form, characterized by chip design & SOT-23 package assembly.

Typical Electrical Characteristics, T_A = 25°C unless otherwise stated

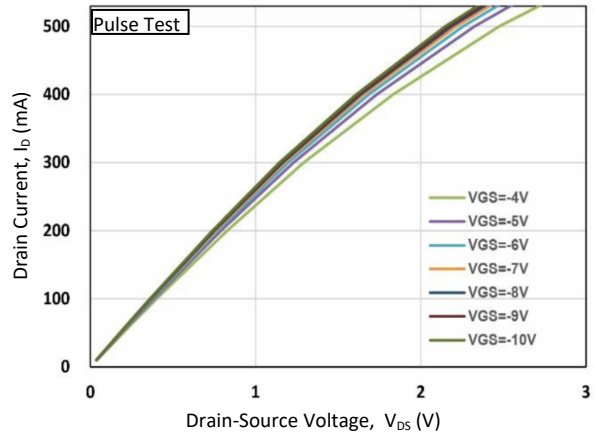


Figure 1 – Drain Current Versus Drain-Source Voltage

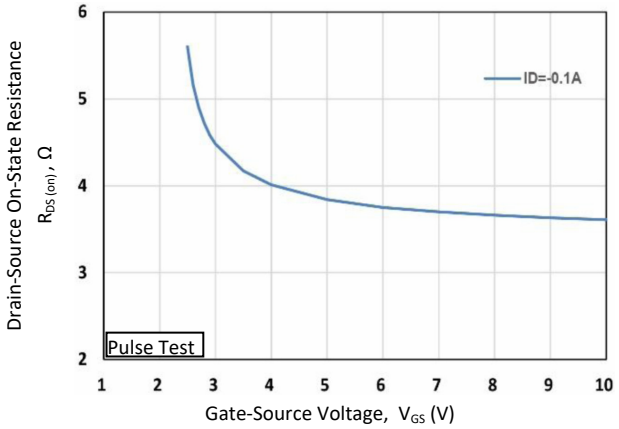


Figure 2 – Drain-Source On-State Resistance Versus Gate-Source Voltage

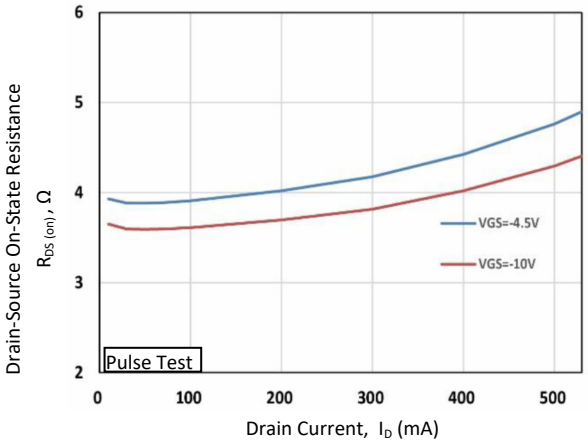


Figure 3 – Drain-Source On-State Resistance versus Drain Current

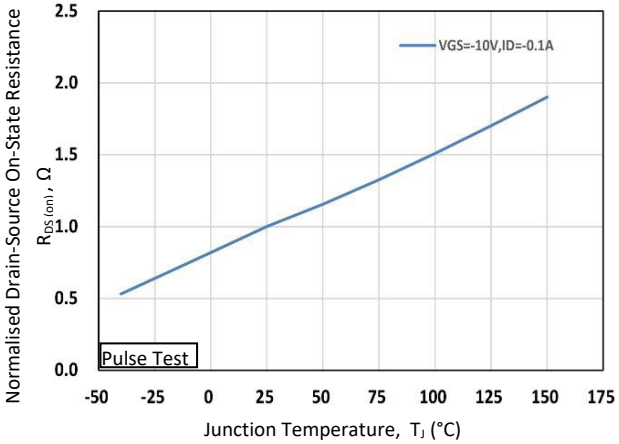


Figure 4 – Normalised Drain-Source On-State Resistance versus Junction Temperature

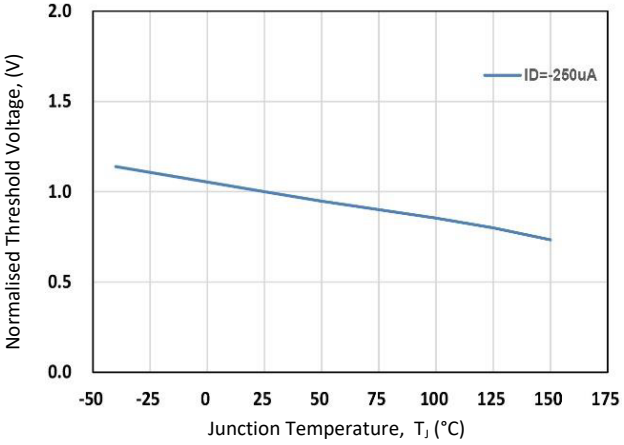


Figure 5 – Normalised Threshold Voltage versus Junction Temperature

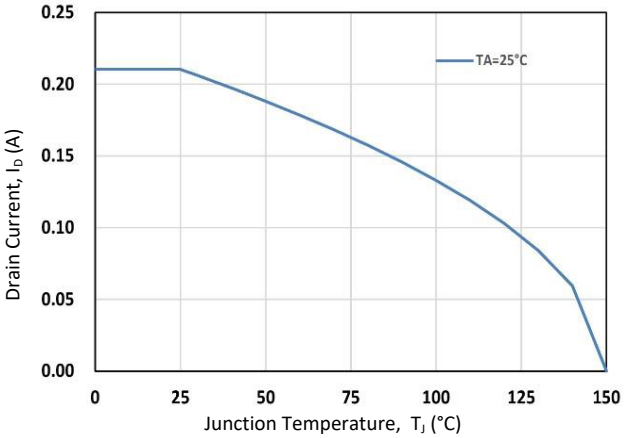


Figure 6 – Drain Current versus Junction Temperature

Typical Electrical Characteristics, T_A = 25°C unless otherwise stated

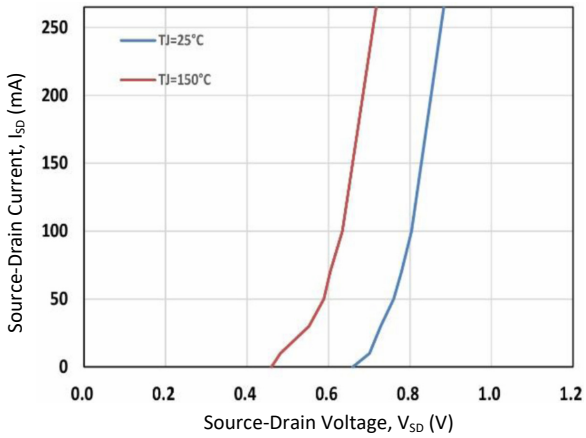


Figure 7 – Body Diode Forward Voltage Versus Source-Drain Current

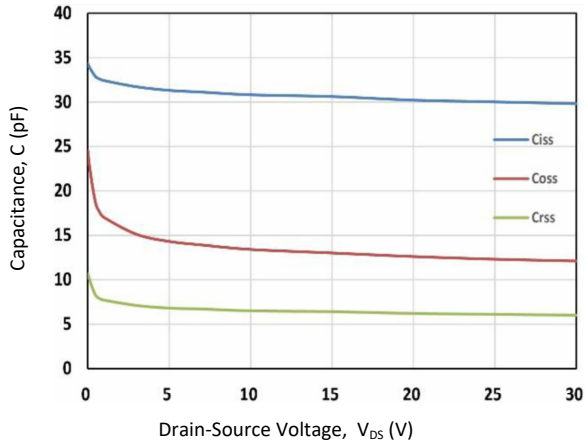


Figure 8 – Capacitance versus Drain-Source Voltage

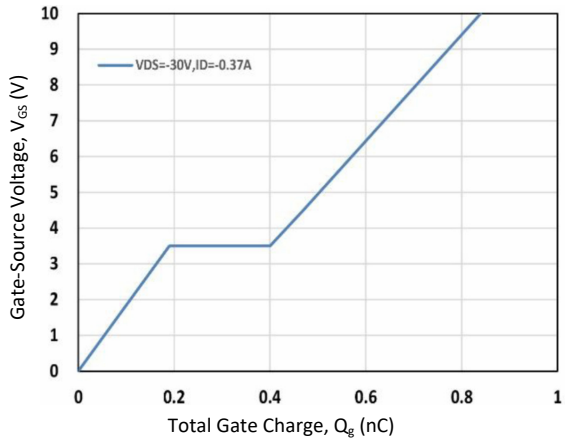


Figure 9 – Gate-Source Voltage versus Total Gate Charge

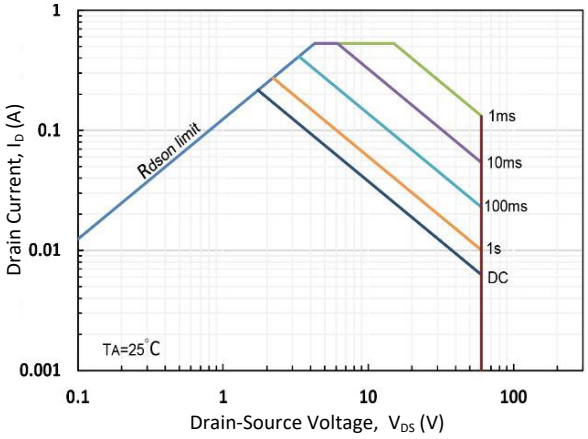


Figure 10 – Safe-Operating-Area

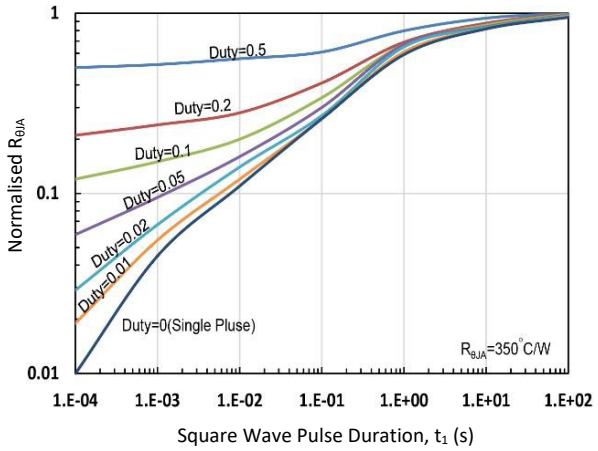


Figure 11– Thermal Resistance versus Pulse Duration

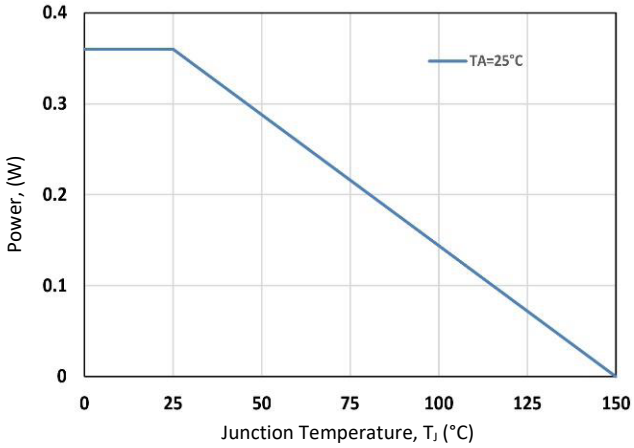


Figure 12– Power Dissipation