



Small Signal MOSFET – SiS60VP02

Rev 1.0
17/06/26

P-Channel Enhancement Mode Field Effect Transistor in bare die form

Features:

- High density cell design for low $R_{DS(ON)}$
- Low Threshold Voltage
- ESD protected Gate
- Suited for High-Speed Switching & Analog Switching
- High Reliability tested grades for Military + Space

Ordering Information:

The following part suffixes apply:

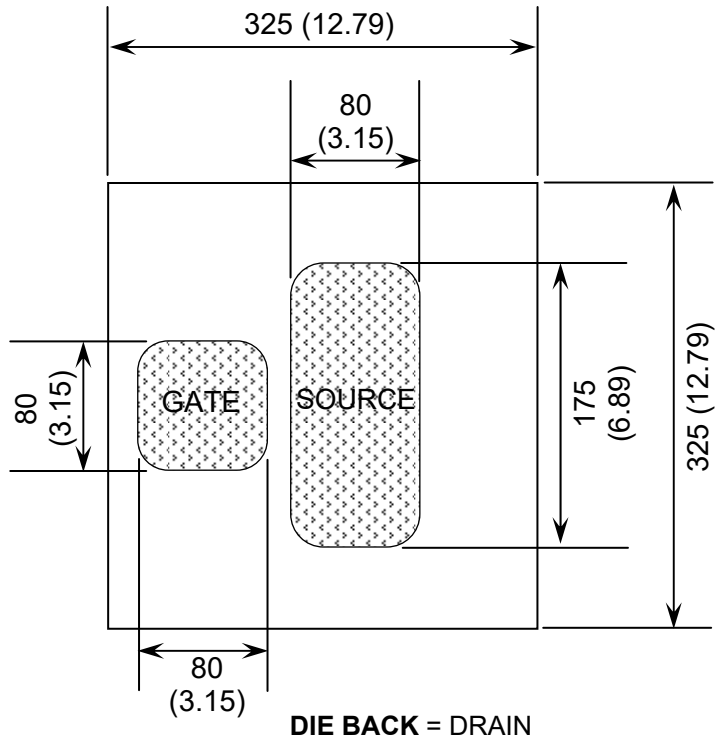
- No suffix - MIL-STD-750 /2072 Visual Inspection
- "H" - MIL-STD-750 /2072 Visual Inspection
+ MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-750 /2072 Visual Inspection
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in μm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- With additional electrical selection – On request
- Sawn as pairs or adjacent pair pick – On request
- Assembled in package – On request

Mechanical Specification

Die Size (Including Saw Street)	325 x 325 12.79 x 12.79	μm mils
Gate Pad Size	80 x 80 3.15 x 3.15	μm mils
Source Pad Size	80 x 175 3.15 x 6.89	μm mils
Die Thickness	152 (± 10) 6 (± 0.39)	μm mils
Top Metal Composition	Al/Cu	
Back Metal Composition	Ti/Ni/Ag/Sn	





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Absolute Maximum Ratings¹ $T_J = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Drain-to-Source Voltage	V_{DSS}	-60	V
Gate-Source Voltage - Continuous	V_{GSS}	± 20	V
Maximum Drain Current - Continuous	I_D	-210	mA
Maximum Drain Current - Pulsed		-530	
Maximum Power Dissipation Derated above 25°C^2	P_D	360	mW
THERMAL CHARACTERISTICS			
Junction & Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance, Junction to Ambient ^{2,3}	$R_{\theta JA}$	350	$^\circ\text{C/W}$

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Die level performance dependent on assembly method & substrate choice 3. SOT-23 package mounted on 1in² FR-4 board with 1oz pin.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48V, V_{GS} = 0$	-	-	-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 10	
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.0	-1.6	-2.5	V
Static Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -100\text{mA}$	-	4.0	6.0	Ω
		$V_{GS} = -4.5V, I_D = -100\text{mA}$	-	4.5	7.0	
Forward Transfer Admittance	$ Y_{fs} $	$V_{DS} = -5V, I_D = -100\text{mA}$	-	4.4	-	S
DYNAMIC CHARACTERISTICS⁵						
Input Capacitance	C_{iss}	$V_{DS} = -30V, V_{GS} = 0V, f = 1\text{MHz}$	-	30	-	μF
Output Capacitance	C_{oss}		-	12	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -10V, V_{DS} = -30V, I_D = -1A, R_{GEN} = 6\Omega$	-	18.4	-	ns
Rise Time	t_r		-	15.2	-	
Turn-Off Time	$t_{d(off)}$		-	113	-	
Fall Time	t_f		-	41	-	
Total Gate Charge	Q_g	$V_{GS} = -4.5V, V_{DS} = -30V, I_D = -0.37A$	-	0.47	-	nC
		$V_{GS} = -10V, V_{DS} = -30V, I_D = -0.37A$	-	0.84	-	
Gate-Source Charge	Q_{gs}	$V_{GS} = -10V, V_{DS} = -30V, I_D = -0.37A$	-	0.19	-	nC
Gate-Drain Charge	Q_{gd}		-	0.21	-	
SOURCE-DRAIN BODY DIODE CHARACTERISTICS						
Diode Forward Voltage ⁴	V_F	$I_F = -0.1A, V_{GS} = 0V$	-	-0.8	-1.1	V
Reverse Recovery Time	t_{rr}	$I_F = -0.18A, V_R = -30V, di_F/dt = 100A/\mu\text{s}$	-	10	-	ns
Reverse Recovery Charge	Q_{rr}		-	5	-	nC

4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. 5. Not production tested in die form, characterized by chip design & SOT-23 package assembly.





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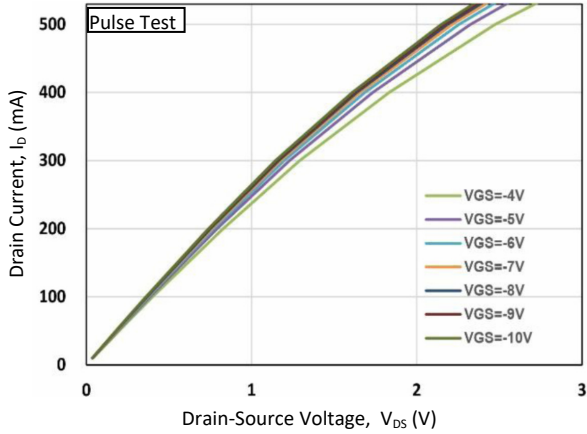


Figure 1 – Drain Current Versus Drain-Source Voltage

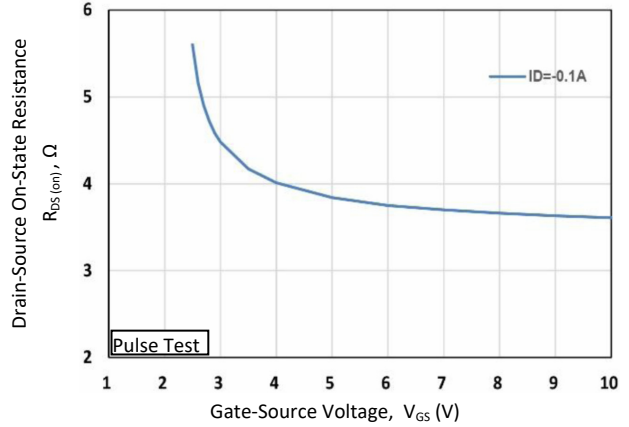


Figure 2 – Drain-Source On-State Resistance Versus Gate-Source Voltage

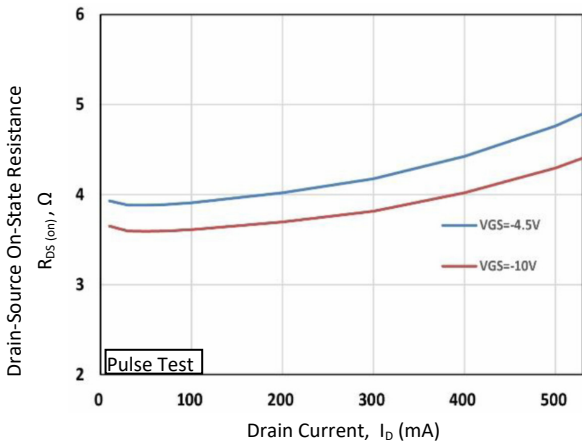


Figure 3 – Drain-Source On-State Resistance versus Drain Current

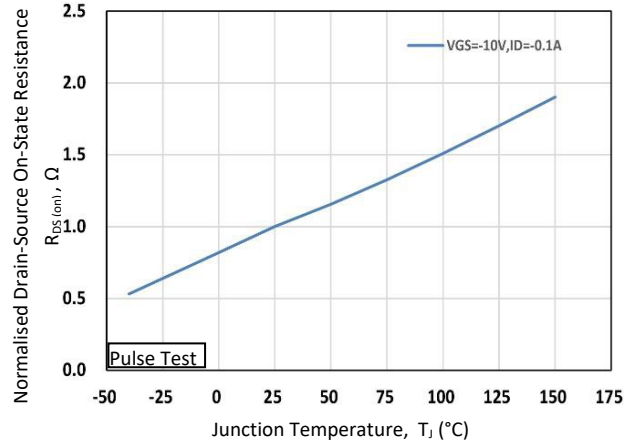


Figure 4 – Normalised Drain-Source On-State Resistance versus Junction Temperature

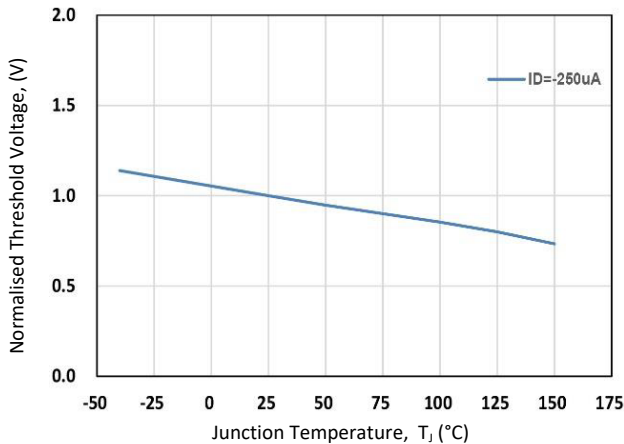


Figure 5 – Normalised Threshold Voltage versus Junction Temperature

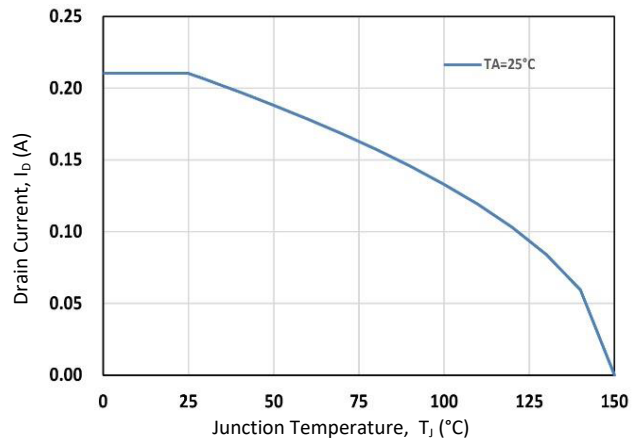


Figure 6 – Drain Current versus Junction Temperature





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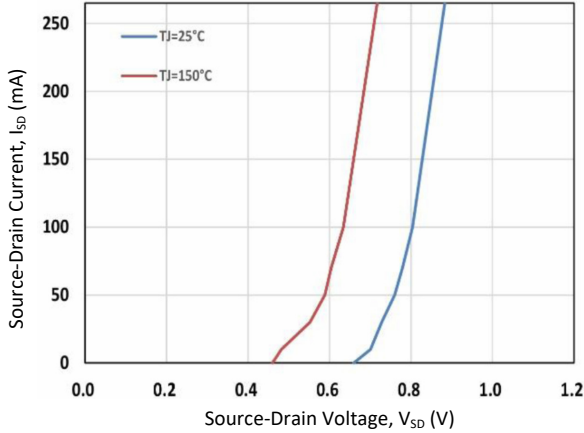


Figure 7 – Body Diode Forward Voltage Versus Source-Drain Current

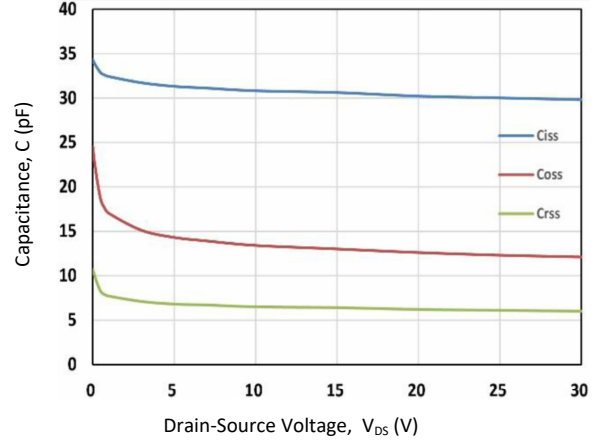


Figure 8 – Capacitance versus Drain-Source Voltage

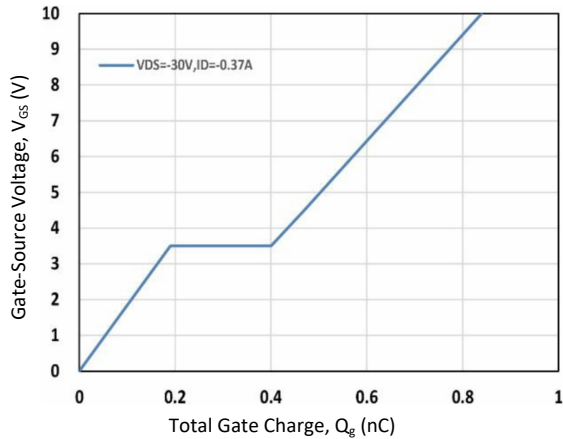


Figure 9 – Gate-Source Voltage versus Total Gate Charge

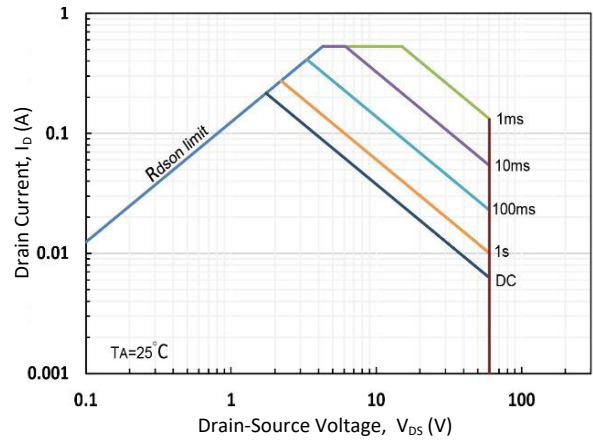


Figure 10 – Safe-Operating-Area

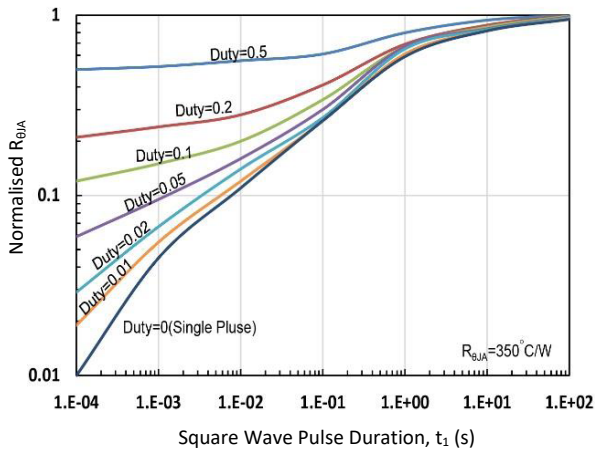


Figure 11– Thermal Resistance versus Pulse Duration

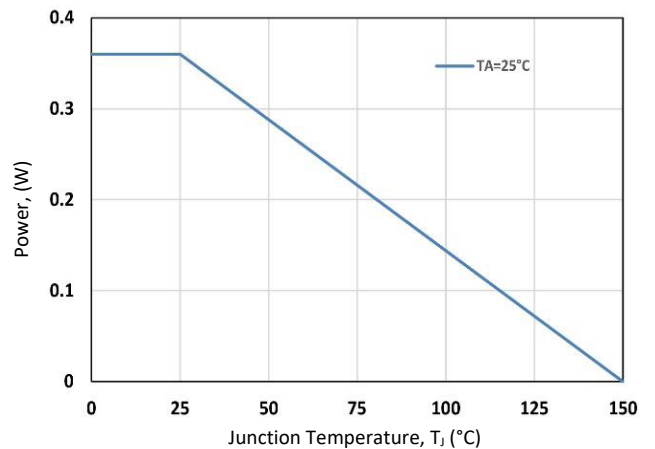


Figure 12– Power Dissipation





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