N-Channel MOSFET Driver – SiS4080A

80V/2.6A Peak, High Frequency Full Bridge MOSFET Driver in bare die form

Rev 1.1
02/09/19

Description

This N-Channel MOSFET driver combines an input comparator to facilitate "hysteresis" with PWM operation to drive high frequency Full Bridge / H-Bridge topologies. A HEN (high enable) signal freewheels current in the lower MOSFETs whilst maintaining the upper MOSFETs in off state. Switching frequency >1MHz enables efficient drive of Switching Power Supplies, Switching Amplifiers & Voice Coil Motors. A single device can drive medium voltage brush motors & x2 devices can drive high performance stepper motors by translating short minimum "on-time" into precision micro-step capability. Propagation delays of ~55ns allow maximum calibration of control loop crossover frequency & dead-time, which adjusts close to zero for minimal distortion & precision load control.

Produced using a unique SOI (Silicon-On-Insulator) design, this device is a ruggedized electrical upgrade of the industry standard HIP4080A. The SiS4080A is specified for high performance & stability under temperature.

Features:

- Latchup free operation via all-around dielectric isolation
- Reduced leakage current & parasitic capacitance for improved power consumption & higher speed
- N-Channel FET full bridge with high side chop capability
- Maximum bootstrap supply voltage 95VDC
- 1000pF load drive at ≥1MHz, t_r / t_f = 10ns
- User-programmable dead time
- Charge-pump & bootstrap maintain upper bias supplies
- DIS (Disable) pin pulls gates low
- Input logic thresholds interface 5V to 15V logic levels
- Very low power consumption
- Under-voltage protection
- Wide automotive temperature range.

Ordering Information

The following part suffixes apply:

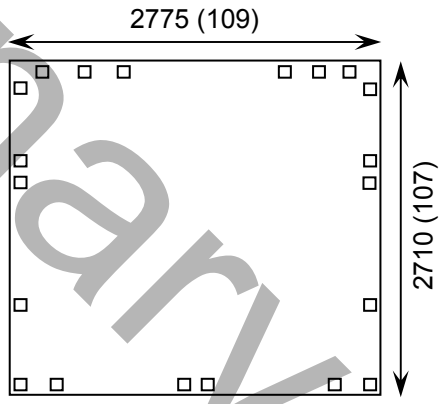
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



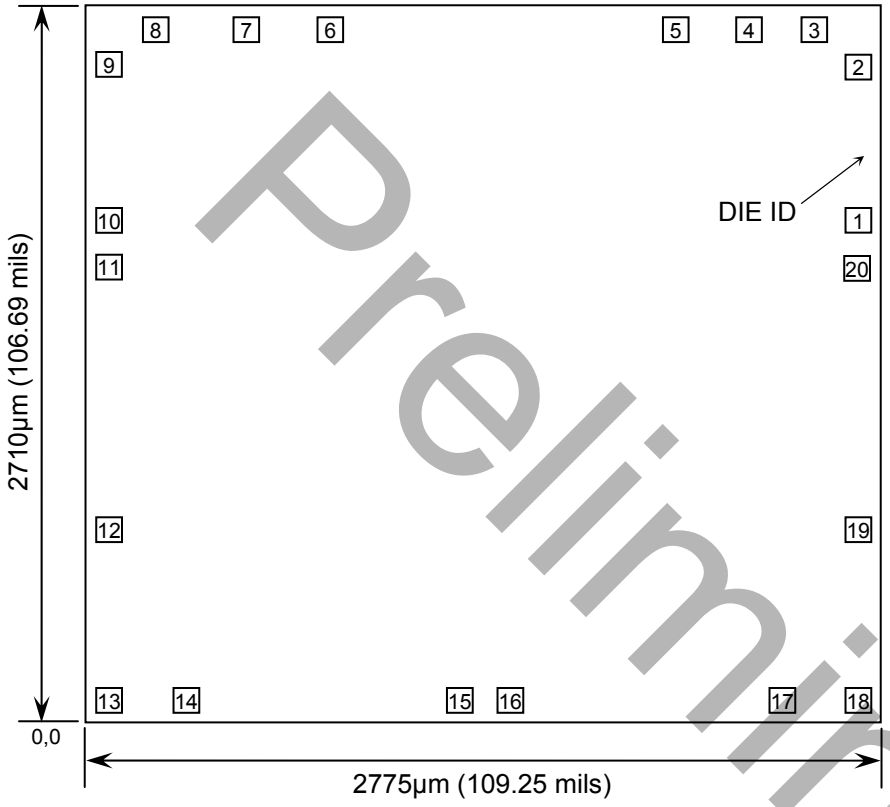
Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into PDIP or SOIC Package – On request

Mechanical Specification

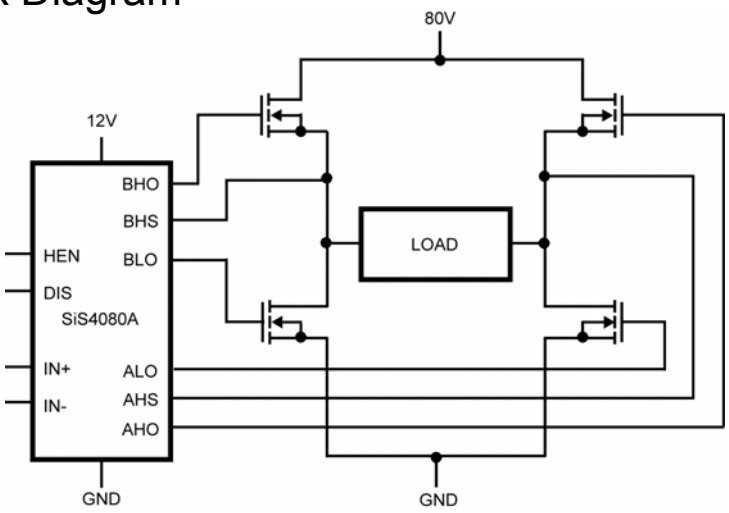
Die Size (Un-sawn)	2775 x 2710 109 x 107	µm mils
Minimum Bond Pad Size	90 x 90 3.54 x 3.54	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	BHB	2648	1858
2	HEN	2648	2435
3	DIS	2485	2581
4	V_{SS}	2263	2581
5	OUT	2011	2581
6	IN+	802	2581
7	IN-	509	2581
8	HDEL	201	2581
9	LDEL	37	2446
10	AHB	37	1858
11	AHO	37	1676
12	AHS	37	682
13	ALO	37	36
14	ALS	304	36
15	V_{CC}	1255	36
16	V_{DD}	1429	36
17	BLS	2380	36
18	BLO	2648	36
19	BHS	2648	682
20	BHO	2648	1676
CHIP BACK IS ISOLATED			

Block Diagram



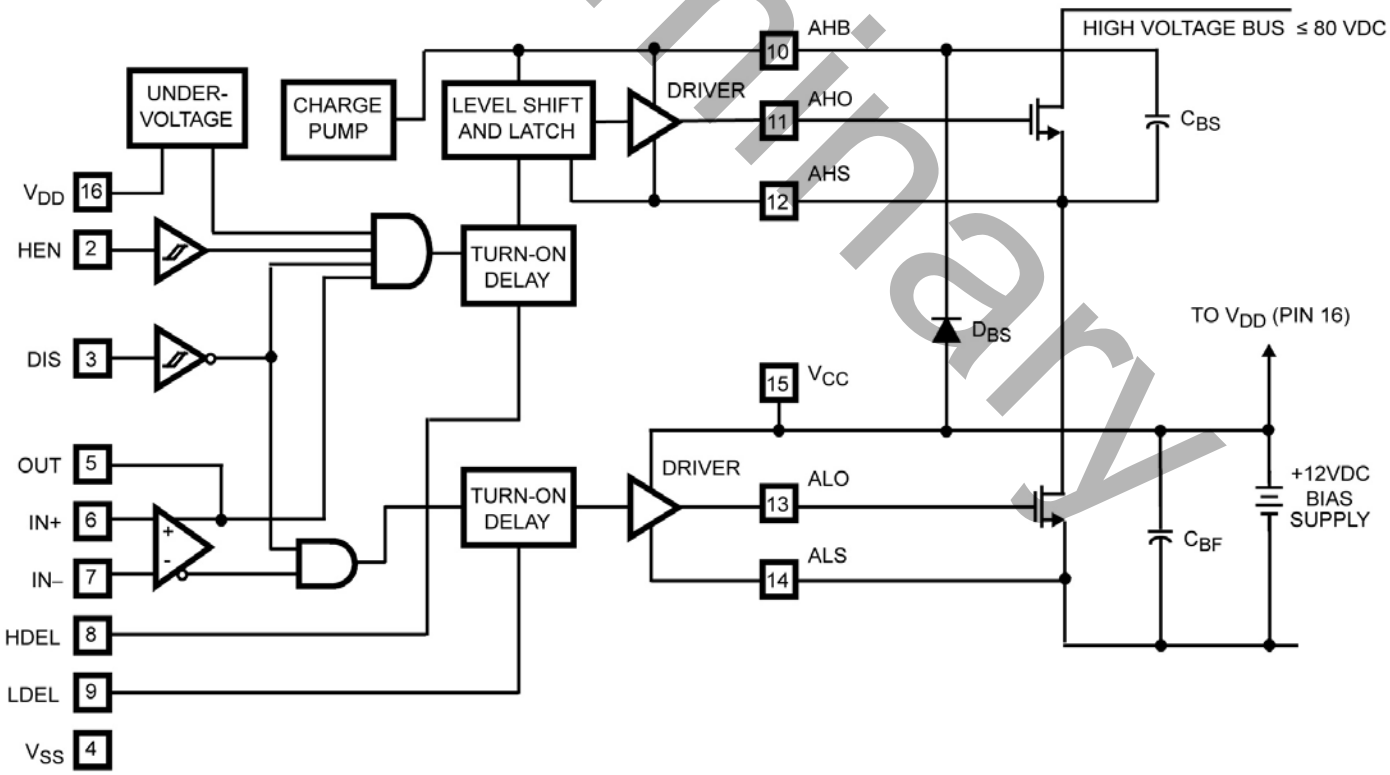
Pad Descriptions

PAD	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pad. Internal charge pump supplies 30µA out of this pad to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
2	HEN	High-side Enable input. Logic level input that when low overrides IN+/IN- (Pads 6 and 7) to put AHO and BHO drivers (Pads 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pad can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pad can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4	V_{SS}	Chip negative supply, generally will be ground.
5	OUT	OUTput of the input control comparator. This output can be used for feedback and hysteresis.
6	IN+	Non-inverting input of control comparator. If IN+ is greater than IN- (Pad 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pad 3) high level will override IN+/IN- control for all outputs. HEN (Pad 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pads 8 and 9).
7	IN-	Inverting input of control comparator. See IN+ (Pad 6) description.
8	HDEL	High-side turn-on DELay. Connect resistor from this pad to V_{SS} to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pad to V_{SS} to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to this pad. Internal charge pump supplies 30µA out of this pad to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 12.8V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pad.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V_{CC}	Positive supply to gate drivers. Must be same potential as V_{DD} (Pad 16). Connect to anodes of two bootstrap diodes.
16	V_{DD}	Positive supply to lower gate drivers. Must be same potential as V_{CC} (Pad 15). De-couple this pad to V_{SS} (Pad 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pad.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

Truth Table

INPUTS				OUTPUTS			
IN+ > IN-	HEN	U/V	DIS	ALO	AHO	BLO	BHO
X	X	X	1	0	0	0	0
0	0	0	0	1	0	0	0
1	1	0	0	0	1	1	0
0	1	0	0	1	0	0	1
1	0	0	0	0	0	1	0
X	X	1	X	0	0	0	0

Functional Block Diagram (1/2 SiS4080A)



Absolute Maximum Ratings[1] (Voltages referenced to V_{SS} unless otherwise stated)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{DD} , V_{CC}	-0.3 to +16	V
Logic I/O Voltages	V_{IN}	-0.3 to V_{DD} +0.3	V
Voltage on AHS, BHS	V_{AHS}, V_{BHS}	-0.6 (transient) to 80V (-55 to +125°C)	V
Voltage on ALS, BLS	V_{ALS}, V_{BLS}	-2.0 (transient) to +2.0 (transient)	V
Voltage on AHB, BHB	V_{AHB}, V_{BHB}	V_{AHS} or V_{BHS} -0.3 to V_{AHS} or V_{BHS} +V_{DD}	V
Voltage on ALO, BLO	V_{ALO}, V_{BLO}	V_{ALS} or V_{BLS} -0.3 to V_{CC} +0.3	V
Voltage on AHO, BHO	V_{AHO}, V_{BHO}	V_{AHS} or V_{BHS} -0.3 to V_{AHB} or V_{BHB} +0.3	V
Input Current, HDEL or LDEL	I_{IN}	-5 to 0	mA
Phase Slew rate	-	20	V/ns
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Junction Temperature	T_J	-40 to 125	°C
Power Dissipation in Still Air[2]	P_D	tbd	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.
2. Measured in package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions (Voltages referenced to V_{SS} unless otherwise stated)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature	T_J	-40	+125	°C
DC Supply Voltage	V_{DD} , V_{CC}	+9.5	+15	V
Voltage on ALS, BLS	V_{ALS}, V_{BLS}	-1.0	+1.0	V
Voltage on AHB, BHB	V_{AHB}, V_{BHB}	V_{AHS} or V_{BHS} +5	V_{AHS} or V_{BHS} +15	V
Input Current, HDEL or LDEL	I_{IN}	-500	-50	µA

DC Electrical Characteristics

V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V, R_{HDEL} = R_{LDEL} = 100K, T_J = -40 to +125°C

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
SUPPLY CURRENTS AND CHARGE PUMPS						
V_{DD} Quiescent Current	I_{DD}	IN- = 2.4V, Other inputs = 0V	8	11	14	mA
V_{DD} Operating Current	I_{DDO}	Outputs switching f = 500kHz, No load	9	12	15	
V_{CC} Quiescent Current	I_{CC}	IN- = 2.4V, Other inputs = 0V I_{ALO} = I_{BLO} = 0	-	25	80	µA
V_{CC} Operating Current	I_{CCO}	f = 500kHz, No load	1	1.25	2.0	mA

DC Electrical Characteristics continued

V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V, R_{HDEL} = R_{LDEL} = 100K, T_J = -40 to +125°C

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
AHB, BHB Quiescent Current – Qpump Output Current	I_{AHB}, I_{BHB}	IN- = 2.5V, Other inputs = 0V, I_{AHO} = I_{BHO} = 0, V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 10V	-50	-25	-11	µA
AHB, BHB Operating Current	I_{AHBO}, I_{BHBO}	f = 500kHz, No load	0.62	1.2	1.5	mA
AHS, BHS, AHB,BHB Leakage Current	I_{HLK}	V_{BHS} = V_{AHS} = 80V, V_{AHB} = V_{BHB} = 93V	-	0.02	1.0	µA
AHS - AHS, BHB - BHS Qpump Output Voltage	V_{AHB} - V_{AHS} V_{BHB} - V_{BHS}	I_{AHB} = I_{BHB} = 0, No Load	11.5	12.6	14.0	V
INPUT COMPARATOR PADS: IN+, IN-, OUT						
Offset Voltage	V_{OS}	Common-mode voltage range	-10	0	+10	mV
Input Bias Current	I_{IB}	-	0	0.5	2	µA
Input Offset Current	I_{OS}	-	-1	0	+1	
Input Common Mode Voltage Range	CMVR	-	1	-	V_{DD} -1.5	V
Voltage Gain	A_{VOL}	-	10	25	-	V/mV
OUT High Level Output Voltage	V_{OH}	IN+ > IN-, I_{OH} = -250µA	V_{DD} -0.4	-	-	V
OUT Low Level Output Voltage	V_{OL}	IN+ < IN-, I_{OL} = +250µA	-	-	0.04	
Low Level Output Current	I_{OL}	V_{OUT} = 6V	6.5	14	19	mA
High Level Output Current	I_{OH}		-17	-10	-3	
INPUT PADS: DIS						
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	
Input Voltage Hysteresis	-	-	-	35	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-130	-100	-75	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	

DC Electrical Characteristics continued

V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V, R_{HDEL} = R_{LDEL} = 100K, T_J = -40 to +125°C

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Low Level Input Voltage	V_{IL}	Full Operating Conditions	-	-	1	V
High Level Input Voltage	V_{IH}	Full Operating Conditions	2.5	-	-	
Input Voltage Hysteresis	-	-	-	35	-	mV
Low Level Input Current	I_{IL}	V_{IN} = 0V, Full Operating Conditions	-260	-200	-150	µA
High Level Input Current	I_{IH}	V_{IN} = 5V, Full Operating Conditions	-1	-	+1	
TURN_IN DELAY PADS: LDEL AND HDEL						
LDEL, HDEL Voltage	V_{HDEL}, V	I_{HDEL} = I_{LDEL} = -100 µA	4.9	5.1	5.3	V
GATE DRIVER OUTPUT PINS: ALO, BLO, AHO AND BHO						
Low Level Output Voltage	V_{OL}	I_{OUT} = 100mA	0.7	0.85	1.0	µA
High Level Output Voltage	V_{CC} - V_{OH}	I_{OUT} = -100mA	0.8	0.95	1.1	
Peak Pull-up Current	I_O+	V_{OUT} = 0V	1.7	2.6	3.8	A
Peak Pull-down Current	I_O-	V_{OUT} = 12V	1.7	2.4	3.3	
Under Voltage, Rising Threshold	UV+	-	8.1	8.8	9.4	V
Under Voltage, Falling Threshold	UV-	-	7.6	8.3	8.9	
Under Voltage, Hysteresis	HYS	-	0.25	0.4	0.65	

AC Electrical Characteristics

V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V, R_{HDEL} = R_{LDEL} = 10K, T_J = -40 to +125°C, C_L = 1000pF

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Lower Turn-off Propagation Delay (IN+/IN- to ALO/BLO)	T_{LPHL}	-	-	40	70	ns
Upper Turn-off Propagation Delay (IN+/IN- to AHO/BHO)	T_{HPHL}	-	-	50	80	

AC Electrical Characteristics continued

V_{DD} = V_{CC} = V_{AHB} = V_{BHB} = 12V, V_{SS} = V_{ALS} = V_{BLS} = V_{AHS} = V_{BHS} = 0V, R_{HDEL} = R_{LDEL} = 10K, T_J = -40 to +125°C, C_L = 1000pF

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Rise Time	T_R	-	-	10	25	ns
Fall Time	T_F	-	-	10	25	
Turn-on Input Pulse Width	TP_{WIN-ON}	-	50	-	-	ns
Turn-off Input Pulse Width	$TP_{WIN-OFF}$	-	40	-	-	
Disable Turn-off Propagation Delay (DIS - Lower Outputs)	T_{DISLOW}	-	-	45	75	ns
Disable Turn-off Propagation Delay (DIS - Upper Outputs)	$T_{DISHIGH}$	-	-	55	85	
Disable to Lower Turn-on Propagation Delay	T_{DLPLH}	-	-	45	70	ns
Refresh Pulse Width (ALO and BLO)	T_{REF-PW}	-	240	380	500	ns
Disable to Upper Enable (DIS - AHO and BLO)	T_{UEN}	-	-	480	630	ns
HEN-AHO, BHO Turn-off, Propagation Delay	$T_{HEN-PHL}$	R_{HDEL} = R_{LDEL} = 10K	-	40	70	ns
HEN-AHO, BHO Turn-on, Propagation Delay	$T_{HEN-PLH}$		-	60	90	ns

Timing Diagrams

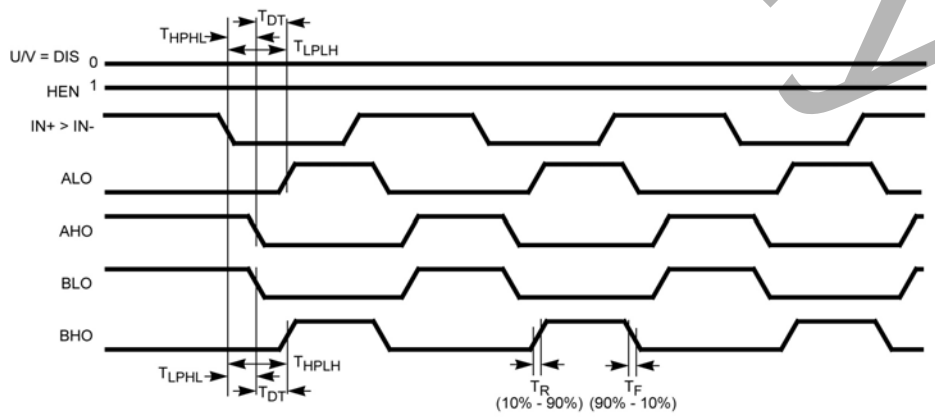


Figure 1 – Bistate Mode

Timing Diagrams continued

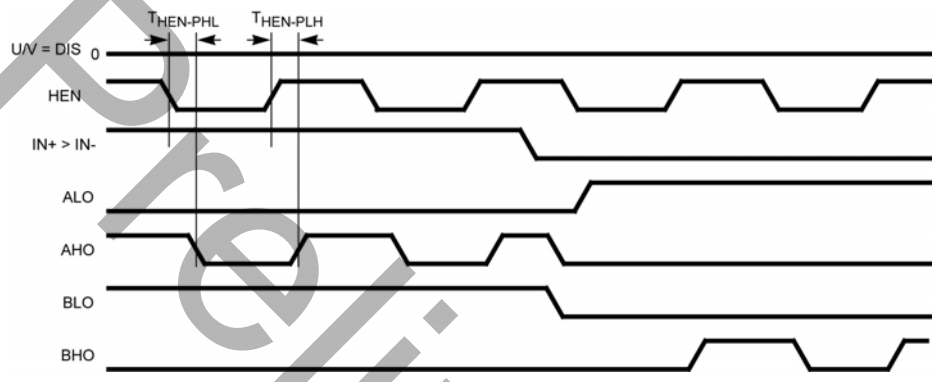


Figure 2 – High-Side Chop Mode

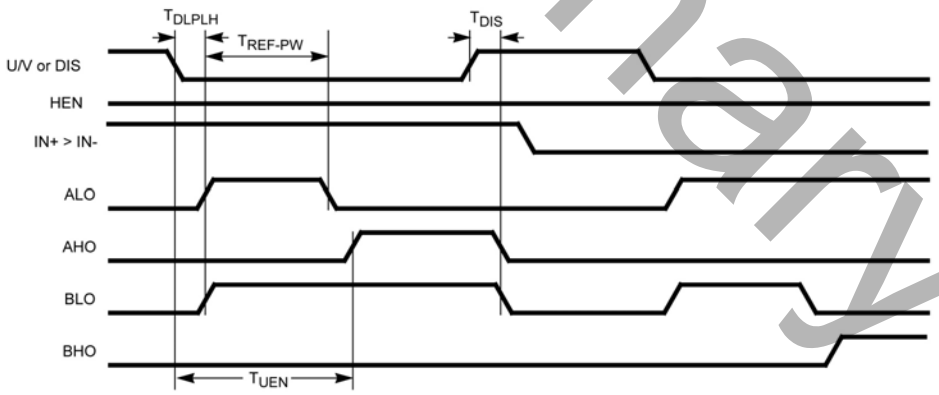


Figure 3 – Disable Function

Typical Application

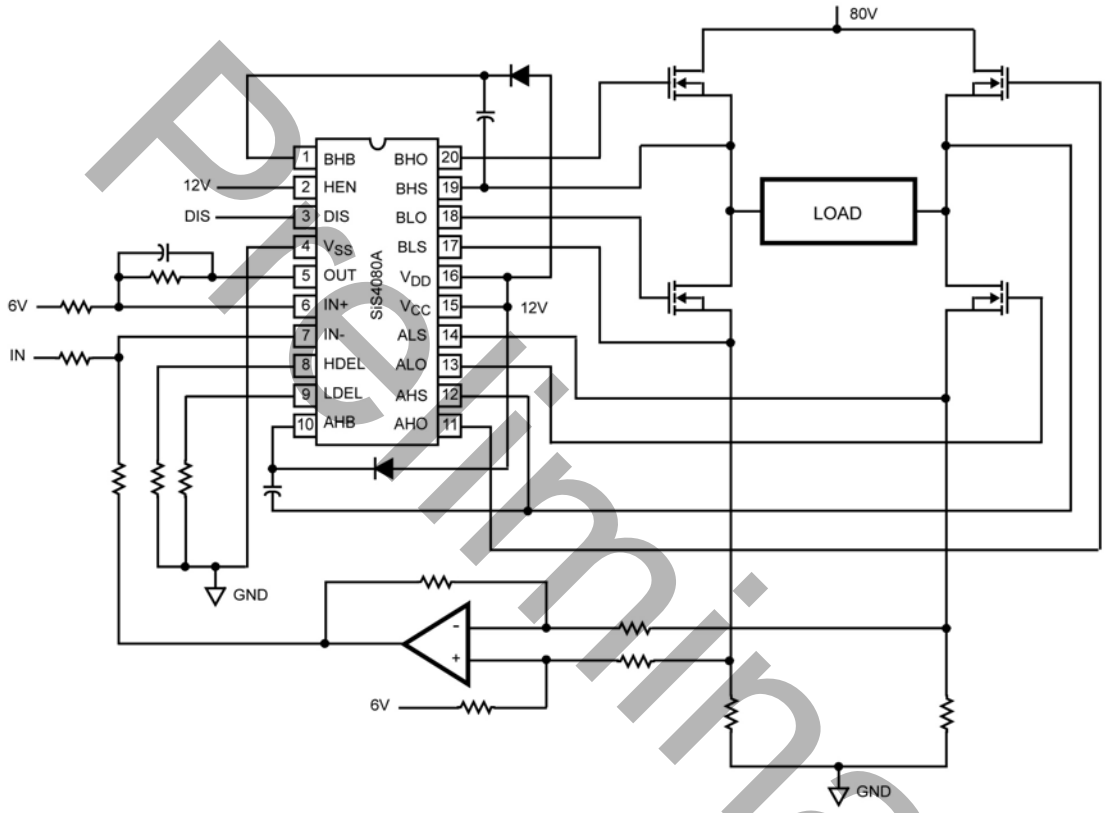


Figure 4 – Hysteresis Mode Switching