Small Signal MOSFET – SiS20VN02

Rev 1.0
07/03/25

N-Channel Enhancement Mode Field Effect Transistor in bare die form

Features:

- High Density Cell Design for Low $R_{DS(ON)}$
- Low Threshold Voltage
- ESD Protected Gate (350V) via Integrated Zener Diode
- Suited for High-Speed Switching & Analog Switching
- High Reliability Tested Grades for Military + Space

Ordering Information:

The following part suffixes apply:

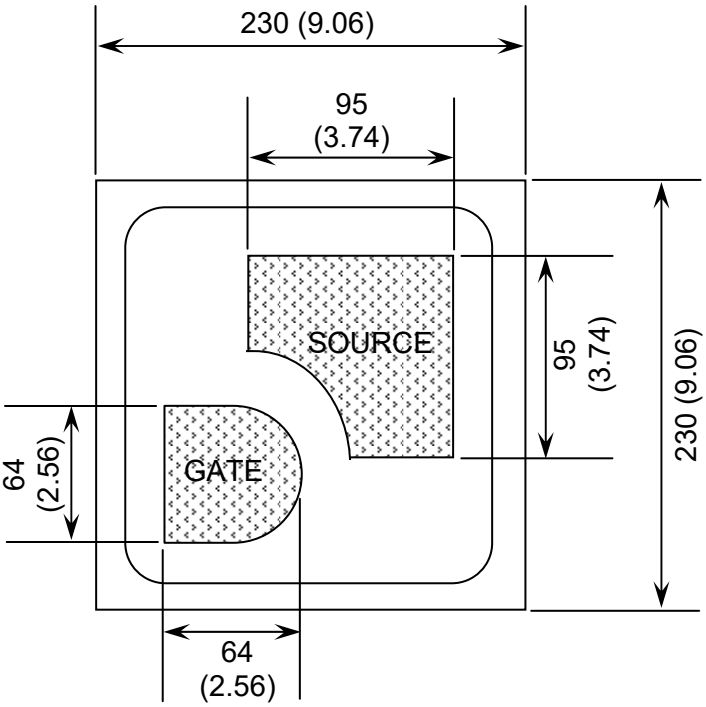
- No suffix - MIL-STD-750 /2072 Visual Inspection
- "**H**" - MIL-STD-750 /2072 Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-750 /2072 Visual Inspection
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



DIE BACK = DRAIN

Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- With additional electrical selection – On request
- Sawn as pairs or adjacent pair pick – On request
- Assembled in package – On request

Mechanical Specification

Die Size (Excluding Saw Street)	230 x 230 9.06 x 9.06	µm mils
Gate Pad Size	64 x 64 2.56 x 2.56	µm mils
Source Pad Size	95 x 95 3.74 x 3.74	µm mils
Die Thickness	100 (±10) 3.94 (±0.39)	µm mils
Top Metal Composition	Al-Si 3.5µm	
Back Metal Composition	Au 1.2µm	

Absolute Maximum Ratings[1] T_J = 25°C unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Drain-to-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage - Continuous	V_{GSS}	±10	V
Maximum Drain Current - Continuous	I_D	230	mA
Maximum Drain Current - Pulsed		920	
Maximum Power Dissipation Derated above 25°C[2]	P_D	300	mW
THERMAL CHARACTERISTICS			
Junction & Storage Temperature	T_J, T_{stg}	-55 to 150	°C
Thermal Resistance, Junction to Ambient[3]	$R_{\theta JA}$	415	°C/W

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Performance at die level dependent on assembly method and substrate choice **3.** Mounted on glass epoxy substrate.

Electrical Characteristics T_J = 25°C unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 100µA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0	-	-	500	nA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 10V, V_{DS} = 0V	-	-	1	µA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -10V, V_{DS} = 0V	-	-	-1	µA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	0.5	-	1.0	V
Static Drain-Source On-Resistance[4]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 100mA	-	1.4	2.5	Ω
		V_{GS} = 2.5V, I_D = 50mA	-	2.2	3.5	
		V_{GS} = 1.8V, I_D = 20mA	-	3.3	5.5	
		V_{GS} = 1.5V, I_D = 10mA	-	4.5	9.5	
		V_{GS} = 1.2V, I_D = 1mA	-	8.6	-	
Forward Transfer Admittance[4]	|Yfs|	V_{DS} = 5V, I_D = 125mA	0.18	26	-	S
Body Diode Forward Voltage	V_F	V_{GS} = 0V, I_F = 10mA	-	0.72	1.0	V
DYNAMIC CHARACTERISTICS[5]						
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	11	-	pF
Output Capacitance	C_{oss}	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	3.6	-	
		V_{DS} = 0V, V_{GS} = 0V, f = 1MHz	-	11.4	-	
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	2.2	-	
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 4.5V, I_D = 0.2A, V_{DD} = 10V	-	8	-	ns
Rise Time	t_r		-	6	-	
Turn-Off Time	$t_{d(off)}$		-	19	-	
Fall Time	t_f		-	11	-	

4. Pulse Test: Pulse width ≤ 80µs, Duty Cycle ≤ 1%. **5.** Not production tested in die form, characterized by chip design & SOT-23 package assembly.

Typical Electrical Characteristics, T_A = 25°C unless otherwise stated

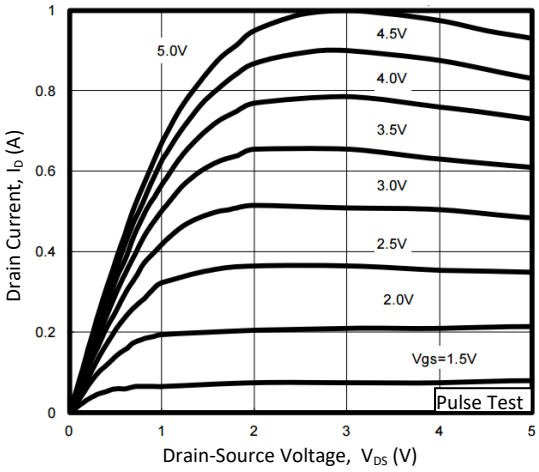


Figure 1 – Drain Current Versus Drain-Source Voltage

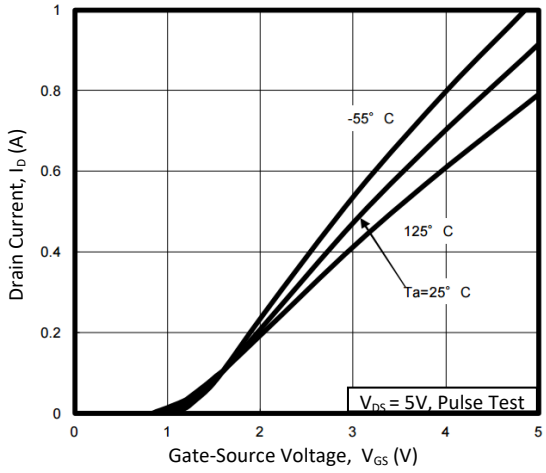


Figure 2 – Drain Current Versus Gate-Source Voltage

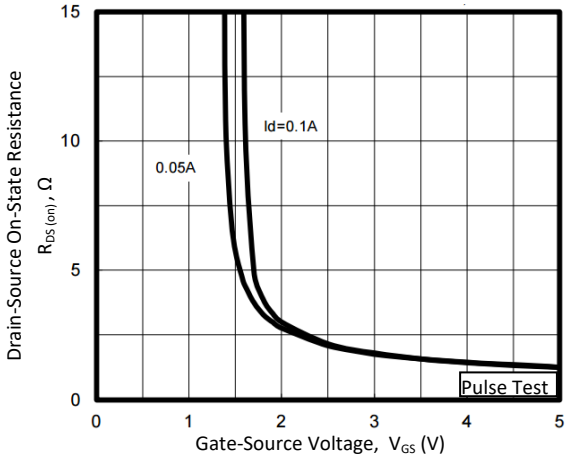


Figure 3 – Drain-Source On-State Resistance Versus Gate-Source Voltage

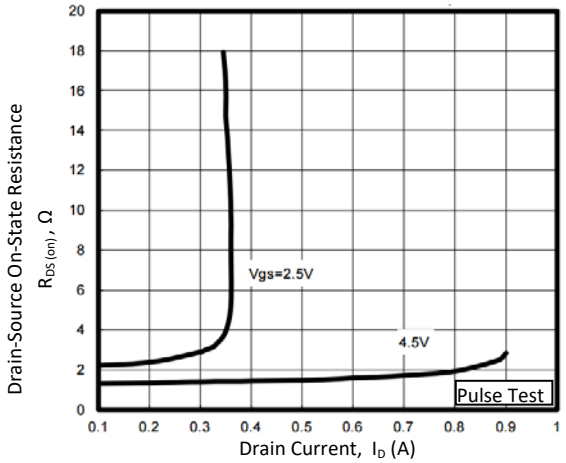


Figure 4 – Drain-Source On-State Resistance versus Drain Current

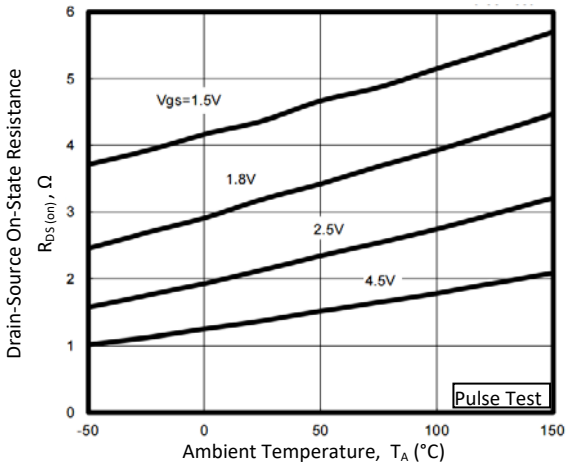


Figure 5 – Drain-Source On-State Resistance versus Ambient Temperature

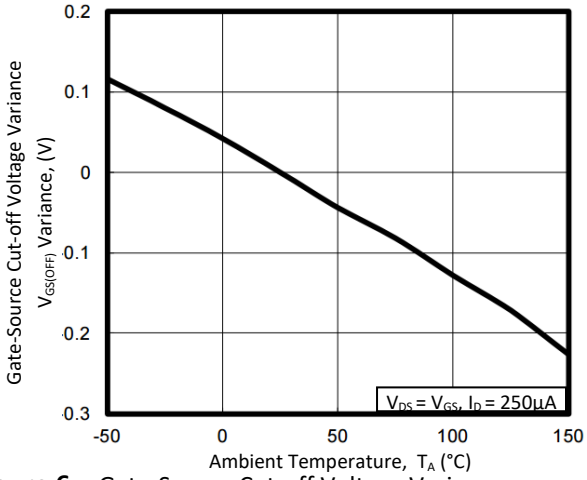


Figure 6 – Gate-Source Cut-off Voltage Variance versus Ambient Temperature

Typical Electrical Characteristics, T_A = 25°C unless otherwise stated

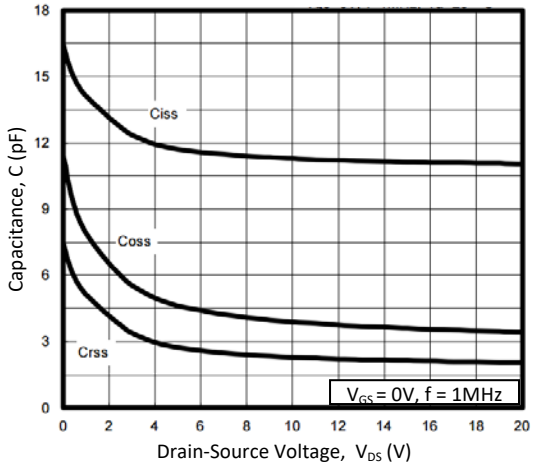


Figure 7 – Capacitance versus Drain-Source Voltage

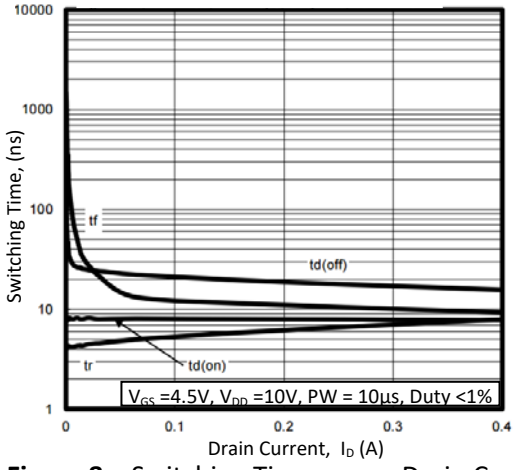


Figure 8 – Switching Time versus Drain Current

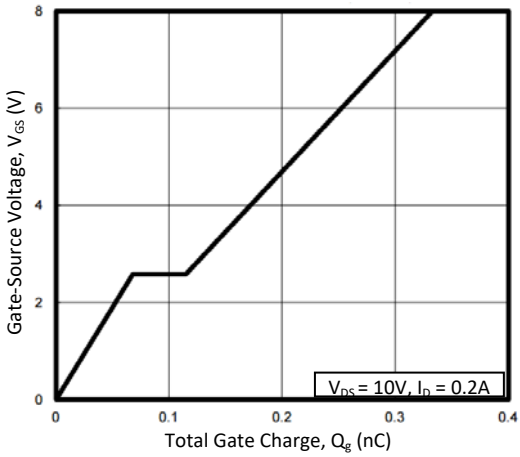


Figure 9 – Gate-Source Voltage versus Total Gate Charge

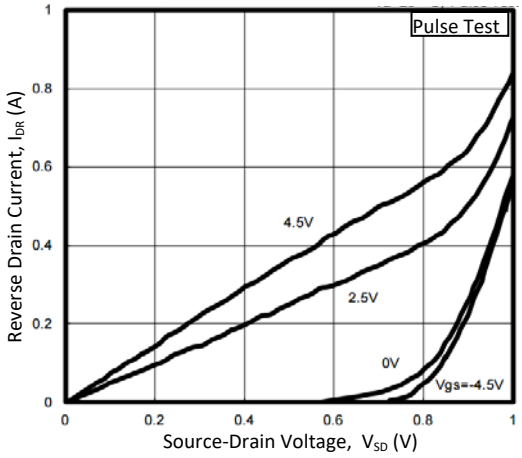


Figure 10 – Reverse Drain Current versus Source-Drain Voltage

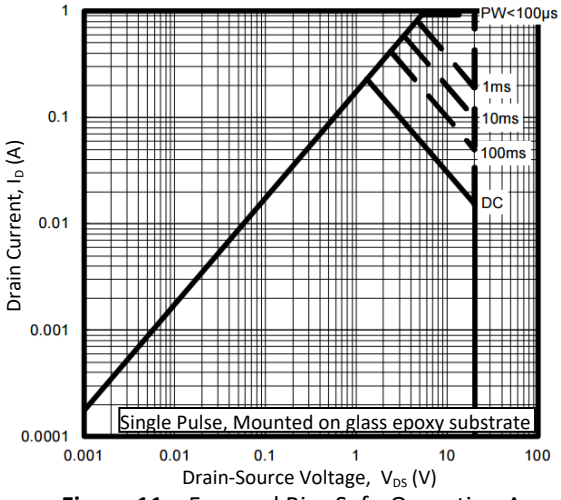


Figure 11 – Forward Bias Safe-Operating-Area

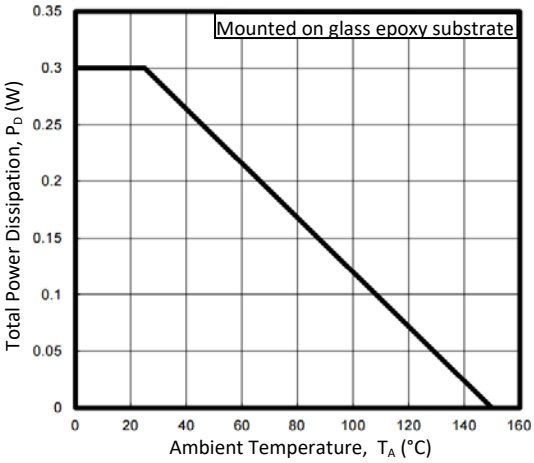


Figure 12 – Total Power Dissipation versus Ambient Temperature

Typical Electrical Characteristics, T_A = 25°C unless otherwise stated

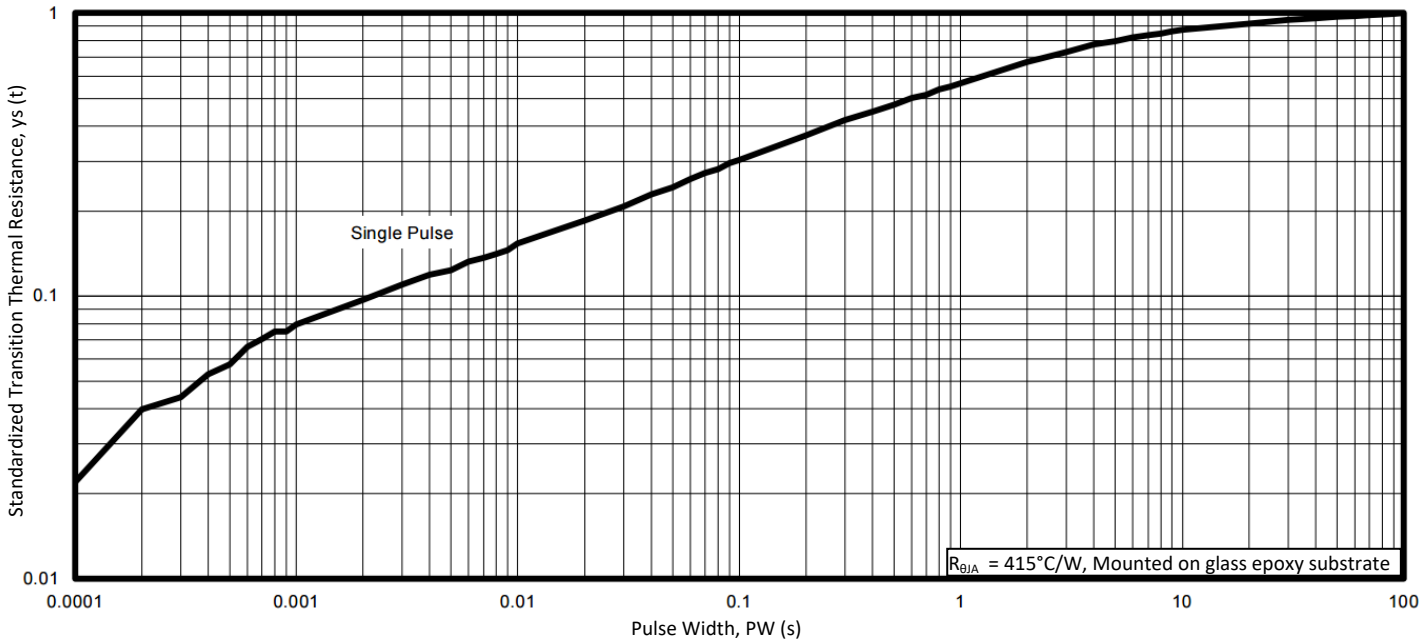


Figure 13 – Standardized Transition Thermal Resistance versus Pulse Width