Dual MOSFET Driver – SiS17601

4A Sink / Source Current, 10ns, Dual MOSFET Driver in bare die form

Rev 1.0
29/01/20

Description

The SiS17601 dual high-speed MOSFET driver sinks / sources up to 4A and finds use in high-frequency circuits due to fast switching time with low propagation delay. Each channel is controlled via non-inverting TTL logic input and enable pins. This device benefits from low input capacitance and drives capacitive load at high speed. Bare die form suits implementation within magnetic environments and in high integration / small size applications.

Applications:

- Power-Supply Modules
- SMPS Power Supplies
- DC-DC Conversion
- Motor Control.

Features:

- Wide single-supply voltage range +4V to +14V
- Input voltage spike protection up to +14V
- Up to 4A peak output current (Sink/Source)
- High speed: 5ns/5ns t_r/t_f typical at 1nF load
- Propagation delay matched between channels
- Low input capacitance: 10pF (typ)
- Thermal shutdown
- Committed long term support with no die mask changes
- Military temperature range.

Ordering Information

The following part suffixes apply:

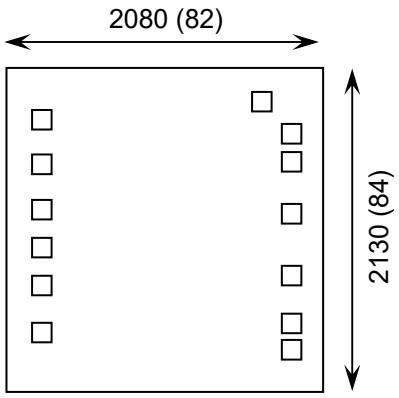
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



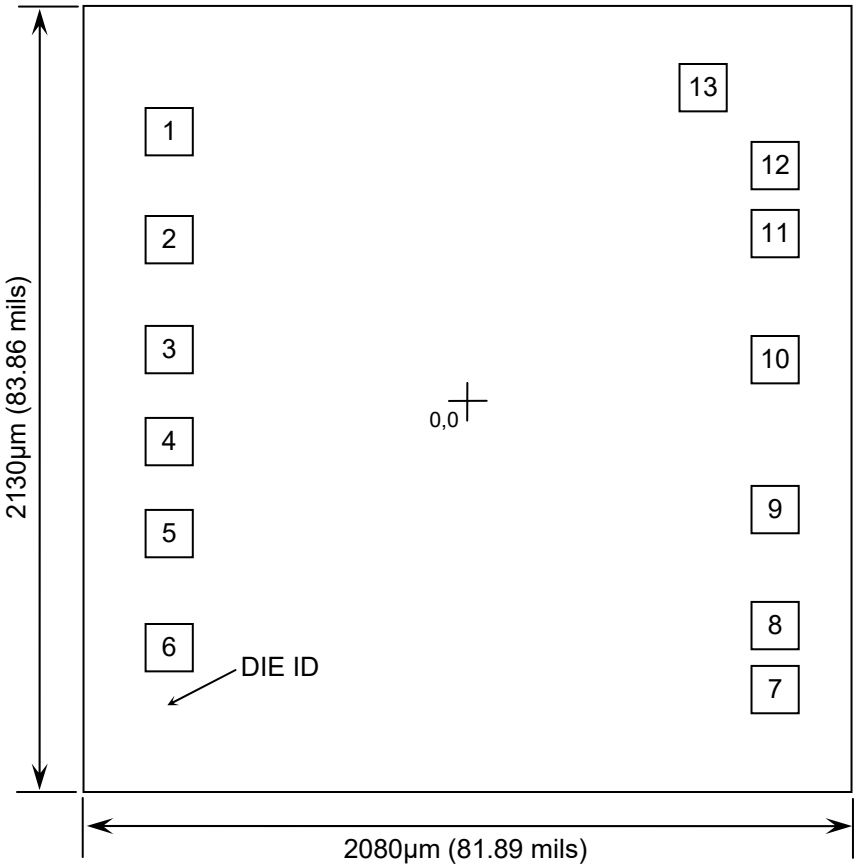
Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 480µm(19 Mils) – On request
- Assembled into PDIP or SOIC Package – On request

Mechanical Specification

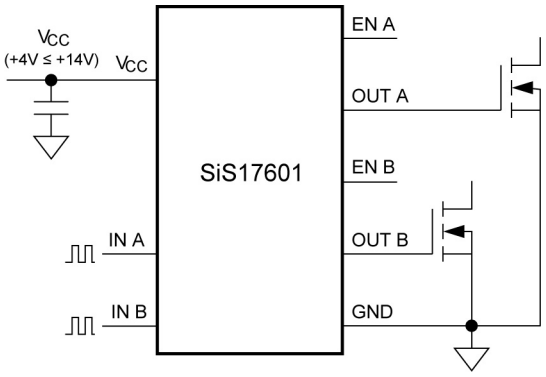
Die Size (Un-sawn)	2080 x 2130 82 x 84	µm mils
Minimum Bond Pad Size	112 x 112 4.40 x 4.40	µm mils
Die Thickness	480 (±20) 19 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	EN A	-816	725
2	IN A	-816	434
3	GND	-816	139
4	GND	-816	-110
5	GND	-816	-363
6	IN B	-816	-673
7	OUT B	816	-783
8	OUT B	816	-611
9	V_{CC}	816	-300
10	V_{CC}	816	107
11	OUT A	816	450
12	OUT A	816	629
13	EN B	622	844
ISOLATE CHIP BACKSIDE			

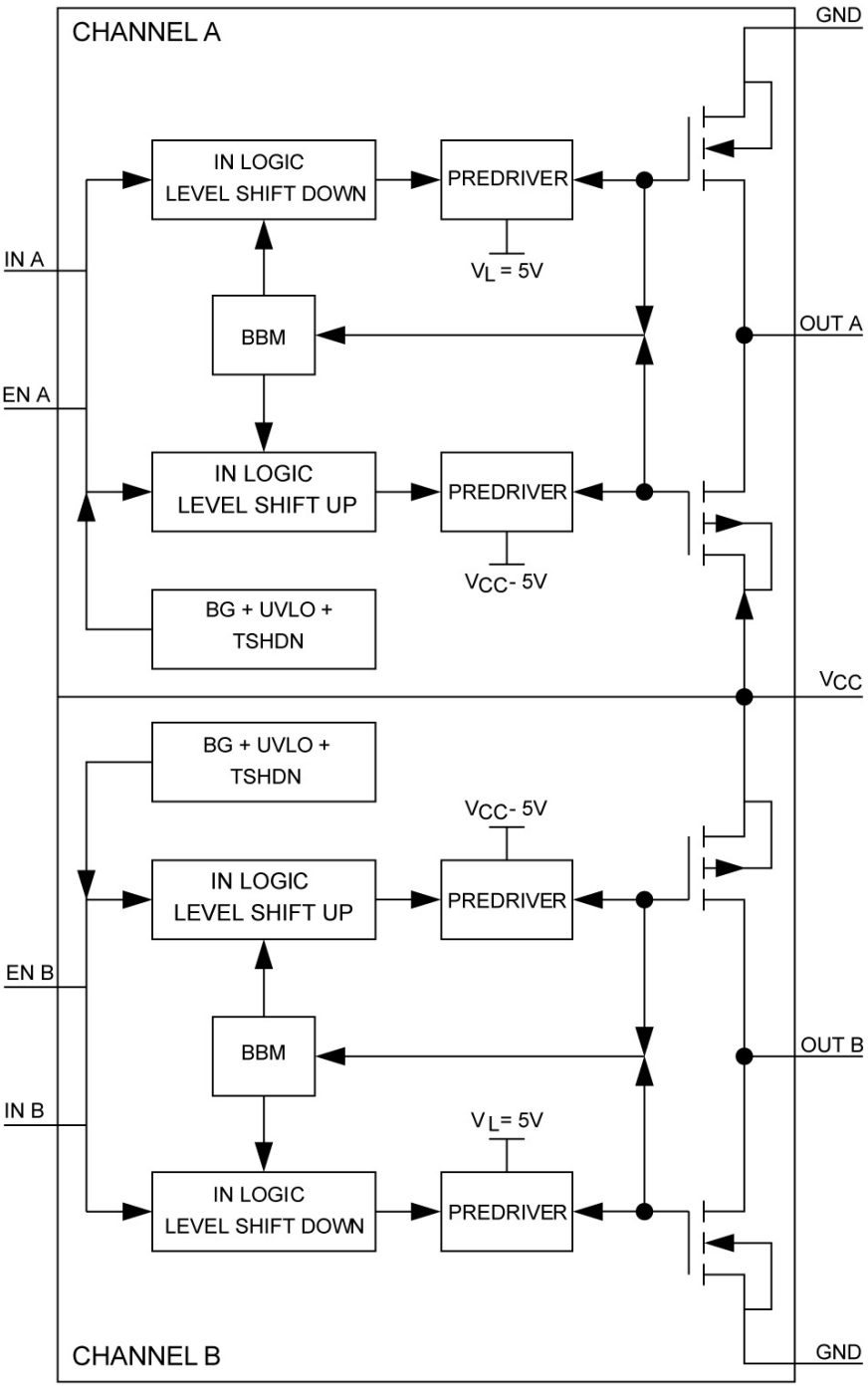
Typical Circuit



Pad Descriptions

PADS	SYMBOL	DESCRIPTION
1	EN A	Enable Input for Driver A. Internally pulled to V_{CC} through a 100kΩ resistor. Leave unconnected for always-on operation. Connect to GND for disabling the corresponding channel.
2	IN A	Logic Input for Channel A
3, 4, 5	GND	Ground
6	IN B	Logic Input for Channel B
7, 8	OUT B	Channel B Driver Output. Sources and sinks current for channel B to turn the external MOSFET at OUT B on or off.
9, 10	V_{CC}	Power-Supply Input. Bypass to GND with one or more low ESR 0.1µF ceramic capacitors.
11, 12	OUT A	Channel A Driver Output. Sources and sinks current for channel A to turn the external MOSFET at OUTA on or off.
13	EN B	Enable Input for Driver B. Internally pulled to V_{CC} through a 100kΩ resistor. Leave unconnected for always-on operation. Connect to GND for disabling the corresponding channel.

Functional Block Diagram



Truth Table

INPUTS				OUTPUTS	
ENABLE		LOGIC			
A	B	A	B	A	B
H	H	H	H	H	H
H	H	H	L	H	L
H	H	L	H	L	H
H	H	L	L	L	L
L	L	X	X	L	L

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Absolute Maximum Ratings[1] (Voltages referenced to GND unless otherwise stated)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.3 to +16	V
Input Voltages IN A, IN B, EN A, EN B	V_{IN}	-0.3 to +16	V
Output Voltages OUT A, OUT B	V_{OUT}	-0.3 to +16	V
Storage Temperature	T_{STG}	-65 to +150	°C
Operating Junction Temperature	T_J	-55 to 125	°C
Power Dissipation[2]	P_D	588	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.
2. Measured in SO package, results in die form are dependent on die attach and assembly method. See also Power Dissipation characteristics.

Recommended Operating Conditions (Voltages referenced to GND unless otherwise stated)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature	T_J	-55	+125	°C
DC Supply Voltage	V_{CC}	+4	+14	V
High-Level Logic Input Voltage	V_{IH}	2.1	-	V
Low-Level Logic Input Voltage	V_{IL}	-	0.8	V

Electrical Characteristics

V_{CC} = 12V, C_L = 0F, T_J = -55 to +125°C unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
POWER SUPPY (V_{CC})							
Operating Range	V_{CC}	-		4	-	14	V
Undervoltage Lockout	UVLO	V_{CC} rising		3	3.5	3.85	V
UVLO Hysteresis	UVLO			-	200	-	mV
UVLO to OUT Delay	UVLO	V_{CC} rising		-	120	-	µs
Supply Current	I_{CC_Q}	Not switching, V_{CC} = 14V		-	1	2	mA
	I_{CC_SW}	V_{CC} = 4.5V, C_L = 1nF, both channels switching at 1MHz		-	10	12	mA
DRIVER OUTPUT (SOURCE / SINK) (OUT A, OUT B)							
Peak Output Current	I_{PK-P}	SOURCE	V_{CC} = 14V, C_L = 10nF	-	4	-	A
	I_{PK-N}	SINK		-	4	-	
Driver Output Resistance, Pulling Up	R_{ON-P}	V_{CC} = 14V, I_{OUT} = 100mA		-	0.70	0.94	Ω
		V_{CC} = 4V, I_{OUT} = 100mA		-	0.88	1.21	

Electrical Characteristics continued

V_{CC} = 12V, C_L = 0F, T_J = -55 to +125°C unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DRIVER OUTPUT (SOURCE / SINK) (OUT A, OUT B)						
Driver Output Resistance, Pulling Down	R_{ON-N}	V_{CC} = 14V, I_{OUT} = -100mA	-	0.70	1.00	Ω
		V_{CC} = 4V, I_{OUT} = -100mA	-	0.80	1.10	
POWER DISSIPATION CALCULATIONS						
GND referenced resistive load	P_D	$P = D \times R_{ON\ (MAX)} \times I_{LOAD}^2$ per channel				
		D = fractional time period output pulls high, R_{ON} = pull-up resistance with output high, I_{LOAD} is output load current of the device				
Capacitive load		$P = C_{LOAD} \times (V_{DD})^2 \times FREQ$ per channel				
		C_{LOAD} = capacitive load, V_{DD} is the supply voltage, FREQ is switching frequency				
LOGIC & ENABLE INPUTS (IN A, IN B, OUT A, OUT B)						

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
LOGIC & ENABLE INPUTS (IN A, IN B, OUT A, OUT B)						
Minimum High-Level Input Voltage	V_{IH}	-	2.1	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-	-	-	0.8	V
Hysteresis Voltage	V_H	-	-	0.34	-	V
Logic Input Leakage Current	I_L	$V_{IN\ A}$ = $V_{IN\ B}$ = 0V or V_{CC}	-1	0.02	1	µA
Logic Input Capacitance	C_{IN}	-	-	10	-	pF
Enable Pullup Resistor to V_{CC}	R_{pu}		50	100	200	kΩ
Propagation Delay, Enable to Output	t_{pd}	Enable Rising	-	7	-	ns
		Enable Falling	-	7	-	
SWITCHING CHARACTERISTICS (V_{CC} = 14V)						
Output A or B, Rise Time	t_R	C_L = 1nF	-	6	-	ns
		C_L = 4.7pF	-	20	-	
		C_L = 10nF	-	40	-	
Output A or B, Fall Time	t_F	C_L = 1nF	-	6	-	ns
		C_L = 4.7pF	-	16	-	
		C_L = 10nF	-	25	-	
Turn-On Delay Time	t_{ON}	C_L = 1nF	-	12	-	ns
Turn-Off Delay Time	t_{OFF}	C_L = 1nF	-	12	-	

Electrical Characteristics continued

V_{CC} = 12V, C_L = 0F, T_J = -55 to +125°C unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
SWITCHING CHARACTERISTICS (V_{CC} = 4.5V)						
Output A or B, Rise Time	t_R	C_L = 1nF	-	5	-	ns
		C_L = 4.7pF	-	15	-	
		C_L = 10nF	-	28	-	
Output A or B, Fall Time	t_F	C_L = 1nF	-	5	-	ns
		C_L = 4.7pF	-	10	-	
		C_L = 10nF	-	18	-	
Turn-On Delay Time	t_{ON}	C_L = 1nF	-	12	-	ns
Turn-Off Delay Time	t_{OFF}	C_L = 1nF	-	12	-	ns
MATCHING CHARACTERISTICS (V_{CC} = 4.5V)						
Matching Propagation Delays,A & B	-	V_{CC} = 14V, C_L = 10nF	-	8	-	ns

Typical Electrical Characteristics

C_L = 1nF, T_J = 25°C unless otherwise noted

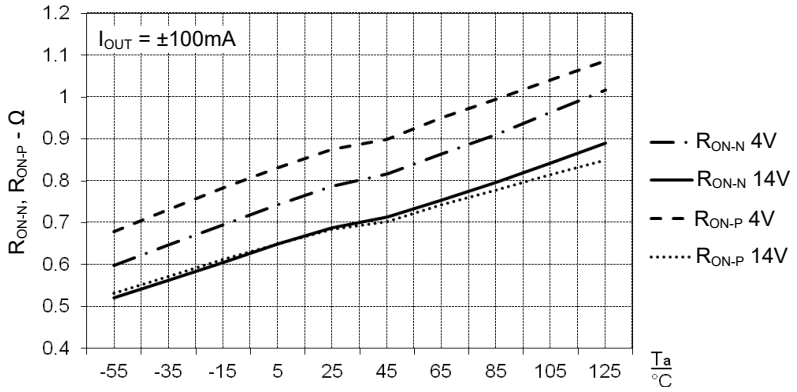


Figure 1 – Output resistance R_{ON-P}, R_{ON-N} Versus Temperature

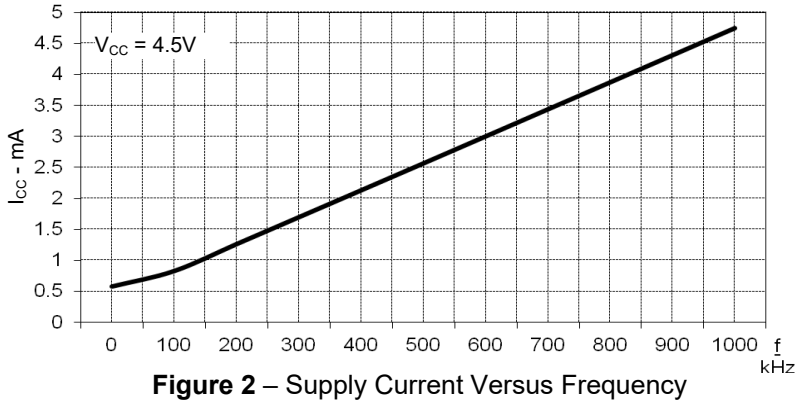


Figure 2 – Supply Current Versus Frequency

Typical Electrical Characteristics continued

C_L = 1nF, T_J = 25°C unless otherwise noted

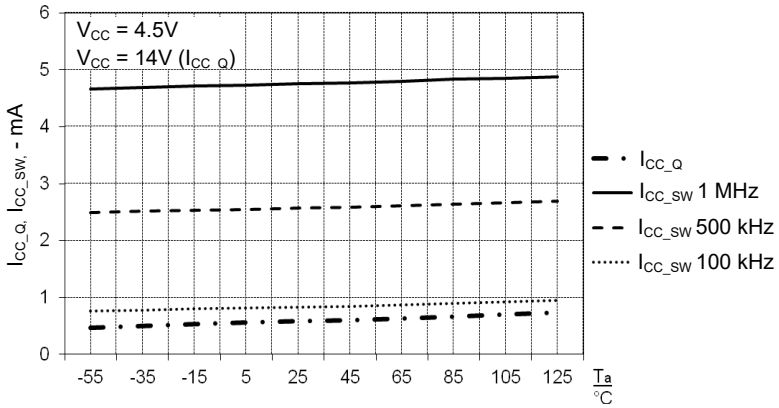
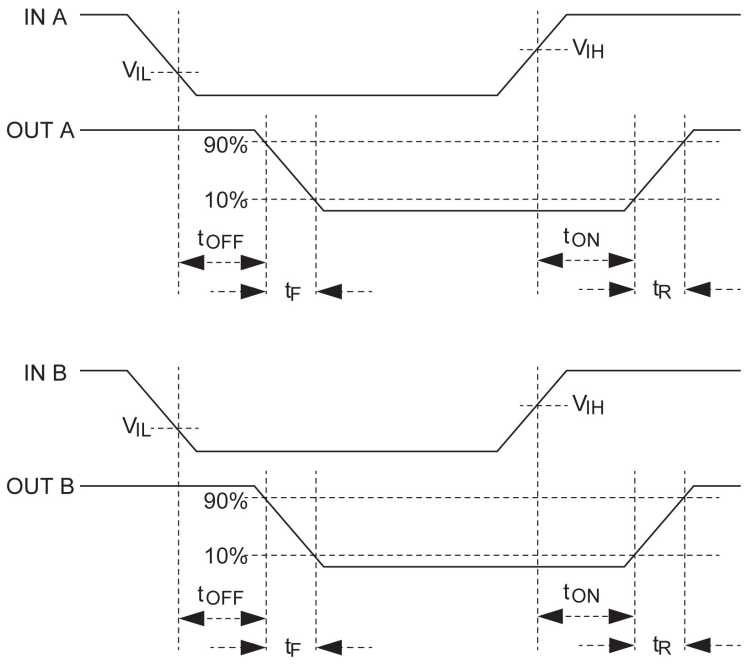


Figure 3 – Supply Current & Dynamic Output Current (One Channel Switching) Versus Frequency

Switching Waveform



Application Notes

Supply Bypassing, Device Grounding, and Placement requirements

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V_{CC} pin can approach 4A, while at the GND pin, the peak current can approach 4A. V_{DD} drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the inverting input is used and the input slew rate is low. The device driving the input should be referenced to the devices' GND pin, especially when the inverting input is used. Ground shifts due to insufficient device grounding can disturb other circuits sharing the same AC ground return path. Any series inductance in the V_{CC}, OUT_, and/or GND paths can cause oscillations due to the very high di/dt that results when the devices are switched with any capacitive load. A 2.2µF or larger value ceramic capacitor is recommended, bypassing V_{CC} to GND and placed as close as possible to the pins. When driving very large loads (e.g., 10nF) at minimum rise time, 10µF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the devices as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

Undervoltage Lockout (UVLO)

When V_{CC} is below the UVLO threshold, the output stage n-channel device is on and the p-channel is off, independent of the state of the inputs. This holds the outputs low. The UVLO is typically 3.6V with 200mV typical hysteresis to avoid chattering. A typical falling delay of 2Fs makes the UVLO immune to narrow negative transients in noisy environments.

Driver Outputs

The devices feature 4A peak sourcing/sinking capabilities to provide fast rise and fall times of the MOSFET gate. Add a resistor in series with OUT_ to slow the corresponding rise/fall time of the MOSFET gate.