JFET Operational Amplifier - SiS1057

Wide bandwidth JFET Input Operational Amplifier in bare die form

Rev 1.0
23/06/18

Description

The SiS1057 JFET input amplifier combines precision specifications with high speed performance. A slew rate of 50V/µs with 1.5 µs settling time to 0.01% is suited for high speed sample + hold circuits and data converters. Low bias current and offset characteristics benefit applications requiring greater precision at speed, such as peak detectors, photodiode amplifiers and log amplifiers. The device exhibits low voltage and current noise at either high or low source impedance. Low drift over temperature delivers improved stability. This device is characterised over the full military temperature range.

Features:

- Wide gain bandwidth: 20MHz (A_V = 5)
- High speed: 50V/µs slew rate, 1.5 µs settling time
- Low noise: 12nv/√Hz (10KHz)
- Low input bias current: 30pA
- Low drift input offset voltage: 1mV, 3µV/°C
- Common-Mode Rejection: 100 dB
- Open-Loop gain: 106 dB
- Differential input voltage range ≤ supply voltage

Ordering Information

The following part suffixes apply:

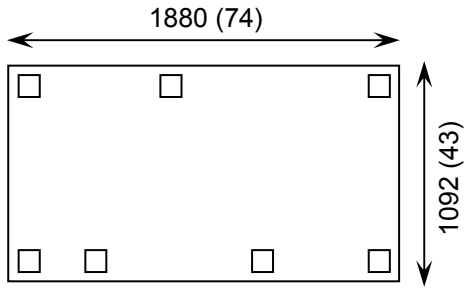
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 460µm(18 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size	1880 x 1092 74 x 43	µm mils
Minimum Bond Pad Size	100 x 100 4 x 4	µm mils
Die Thickness	460 (±20) 18 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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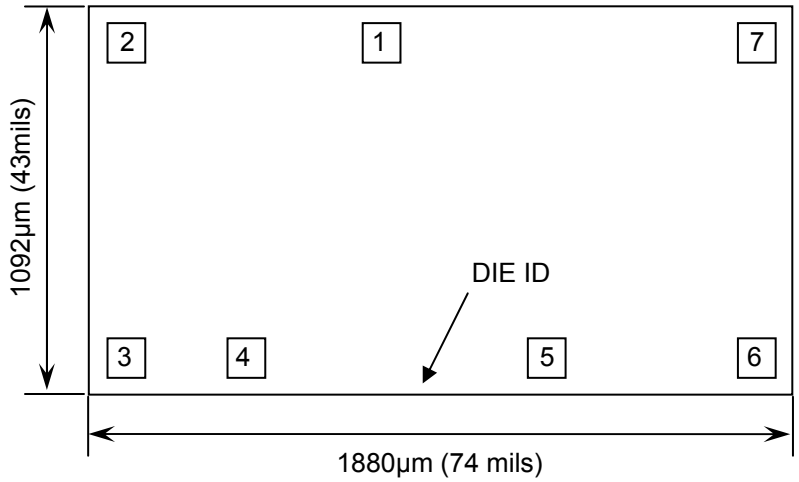
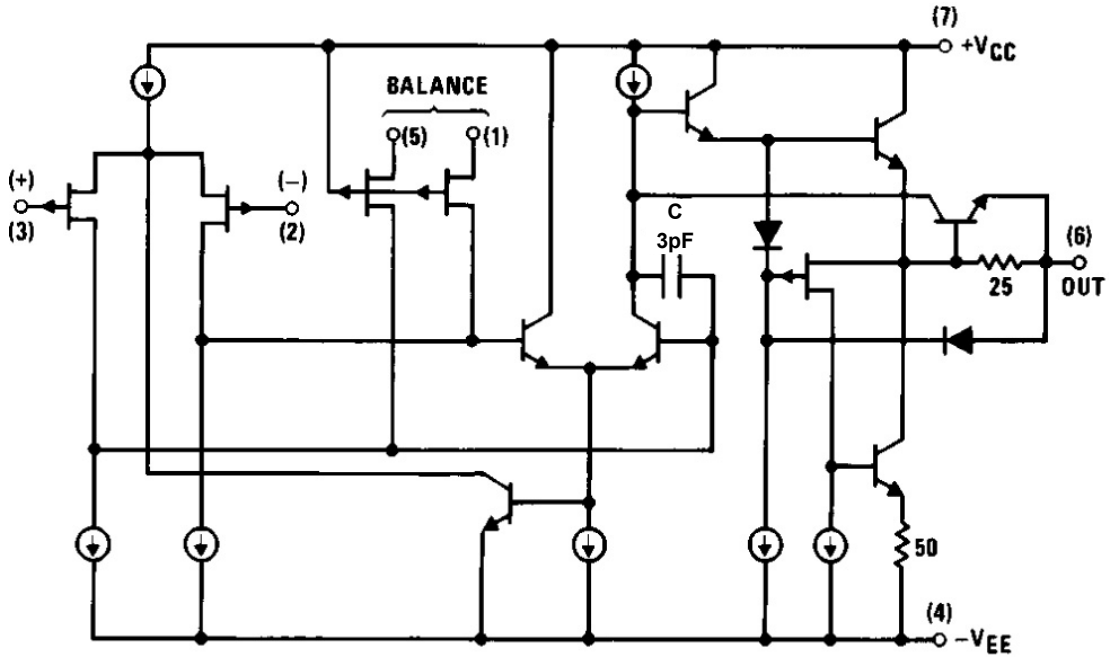
Pad Layout and Functions



PAD	FUNCTION
1	BALANCE
2	IN-
3	IN+
4	V-
5	BALANCE
6	OUTPUT
7	V+
CONNECT CHIP BACK TO V-	

Simplified Schematic



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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_S	±22	V
Input Differential Voltage Range	V_{IDR}	±40	V
Input Voltage Range[2]	V_I	±20	V
Output Short Circuit to Ground	-	Continuous	-
Electrostatic Discharge[3]	V_{ESD}	±1000	V
Power Dissipation in Still Air	P_D	570	mW
Storage Temperature	T_{STG}	-65 to +150	°C
Junction Temperature	T_J	150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. 100 pF discharged through 1.5-kΩ resistor, Human body model (HBM).

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Supply Voltage	V_{CC}	±15	±20	V
Operating Temperature	T_J	-55	+125	°C

DC Electrical Characteristics (-55°C ≤ T_J ≤ +125°C, ±15V ≤ V_S ≤ ±20V unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	R_S = 50Ω, V_{CM} = 0V	25°C	-	1	2	mV
			125°C	-	-	2.5	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S = 50Ω, V_{CM} = 0V		-	3	5	µV/°C
Change in Drift with V_{OS} adjust[4]	$\Delta TC / V_{IO}$			-	0.5	-	µV/°C per mV
Input Offset Current	I_{IO}	V_{CM} = 0V	25°C	-	3	10	pA
			125°C	-	-	10	nA
Input Bias Current[5]	I_{IB}	V_{CM} = 0V	25°C	-	30	50	pA
			125°C	-	-	25	nA
Supply Current	I_{CC}	V_s = ±15V	25°C	-	5	6	mA
Common Mode Input Voltage range	V_{ICR}	V_s = ±15V		±11	+15.1 -12	-	V

4. Temperature Coefficient of the adjusted input offset voltage changes 0.5mV/°C typically for each mV of adjustment from it's original unadjusted value. Common-mode rejection and open loop voltage gain are unaffected by offset adjustment.
5. In normal operation junction temperature rises above ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_J A$, where $\theta_J A$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended to minimalize input bias current.

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DC Electrical Characteristics ($-55°C \le T_J \le +125°C$, $\pm15V \le V_S \le \pm20V$ unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Resistance	R_{IN}	T_J = 25°C		-	10^{12}	-	Ω
Large-Signal Open-Loop Voltage Gain	A_{VOL}	V_S = ±15V, V_O = ±10V, $R_L \ge 2K\Omega$	25°C	50	200	-	V/mV
			125°C	50	-	-	
Output Voltage Swing	V_O	V_S = ±15V, R_L=10KΩ		±12	±13	-	V
		V_S = ±15V, R_L=2KΩ		±10	±12	-	
Common-Mode Rejection Ratio	CMRR			85	100	-	dB
Power Supply Rejection Ratio	PSSR			85	100	-	dB

AC Electrical Characteristics (T_J = 25°C, V_S = ±15V unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Slew Rate	SR	A_V = 5		40	50	-	V/μs
Gain Bandwidth	GBW			15	20	-	MHz
Settling Time	t_s	A_V = -5, 10V Step 0.01%		-	1.5	-	μS
Equivalent Input Noise Voltage	e_n	R_S = 100Ω	f_O = 100Hz	-	15	-	nV/√Hz
			f_O = 1KHz	-	12	-	
Equivalent Input Noise Current	i_n	R_S = 100Ω	f_O = 100Hz	-	0.01	-	pA/√Hz
			f_O = 1KHz	-	0.01		
Input Capacitance	C_{IN}			-	3	-	pF

Typical DC Characteristics

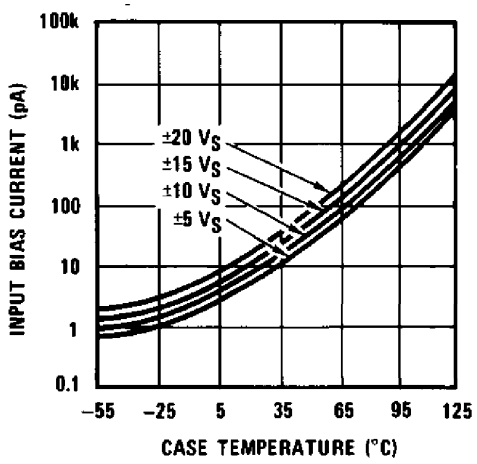

FIGURE 1. Input Bias Current

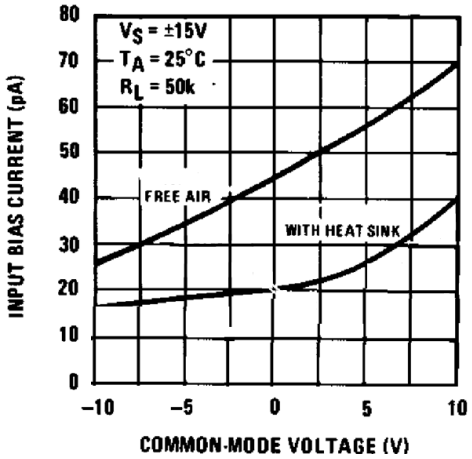

FIGURE 2. Input Bias Current V_{CM}

Typical DC Characteristics continued

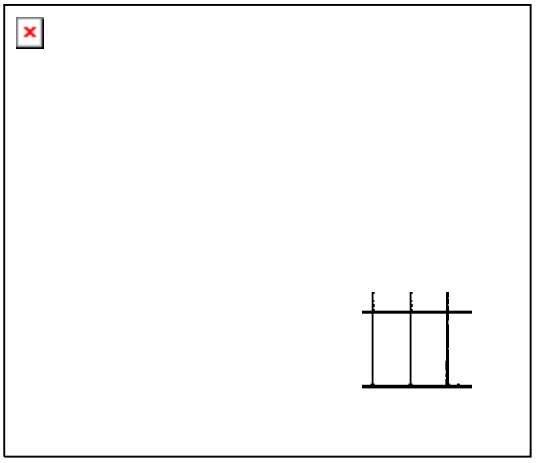

FIGURE 3. Supply Current

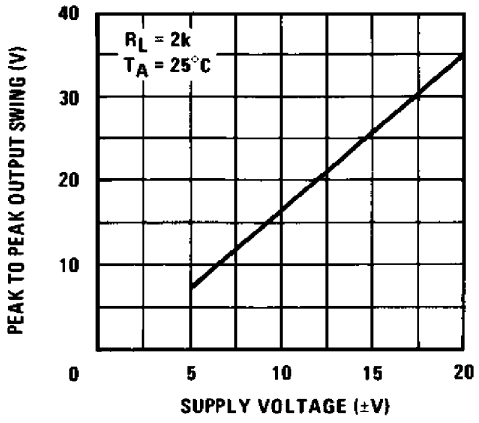

FIGURE 4. Voltage Swing

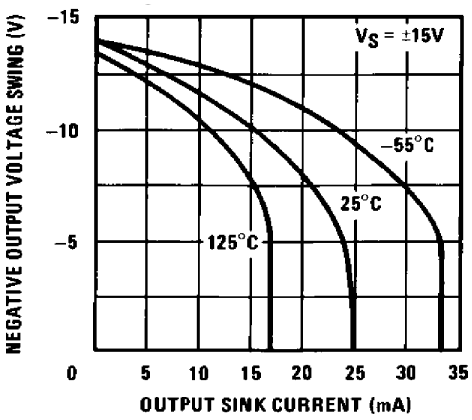

FIGURE 5. Negative Current Limit

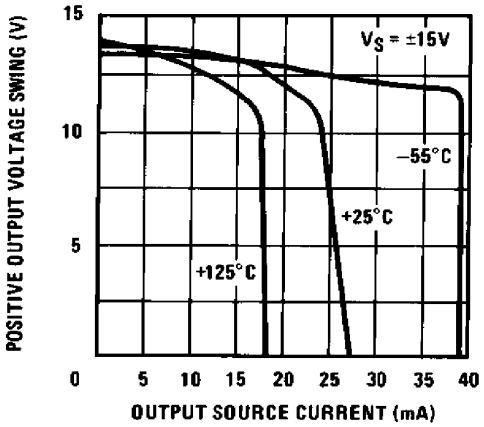

FIGURE 6. Positive Current Limit

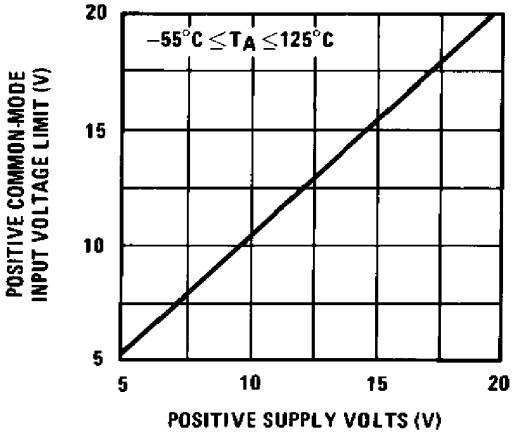

FIGURE 7. Positive Common-Mode Input Voltage Limit

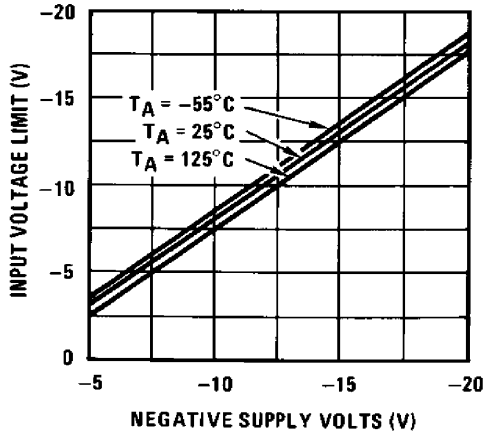

FIGURE 8. Negative Common-Mode Input Voltage Limit

Typical DC Characteristics continued

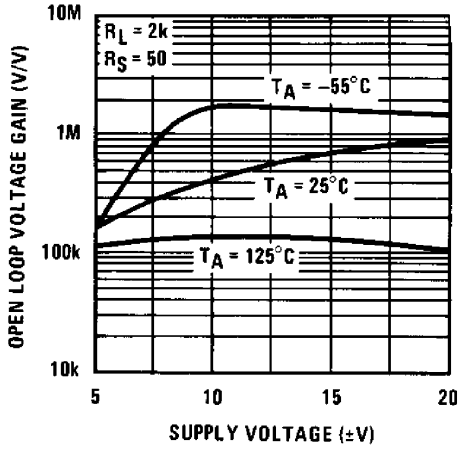

FIGURE 9. Open-Loop Voltage Gain

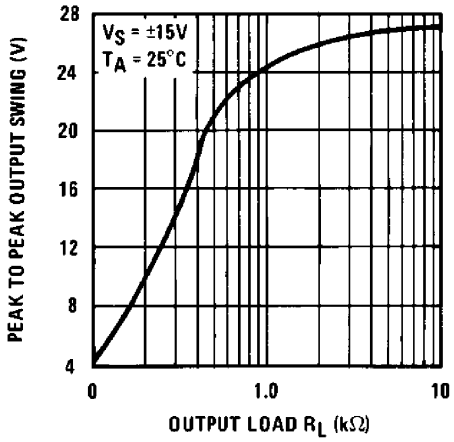

FIGURE 10. Output Voltage Swing

Typical AC Characteristics

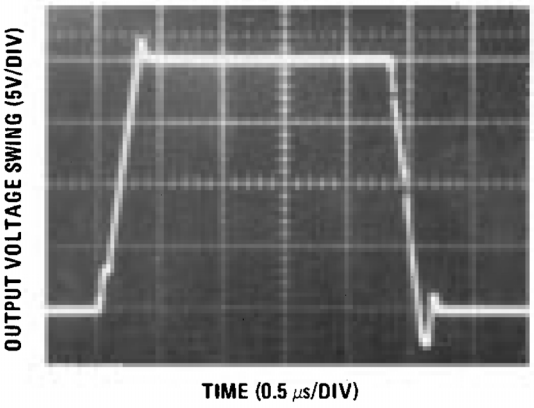

FIGURE 11. Large Signal Pulse Response, A_V = +5

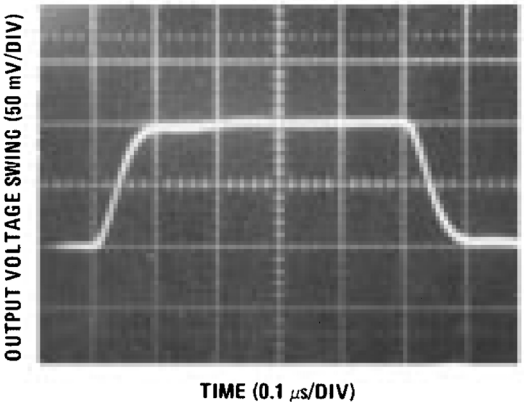

FIGURE 12. Small Signal Pulse Response, A_V = +5

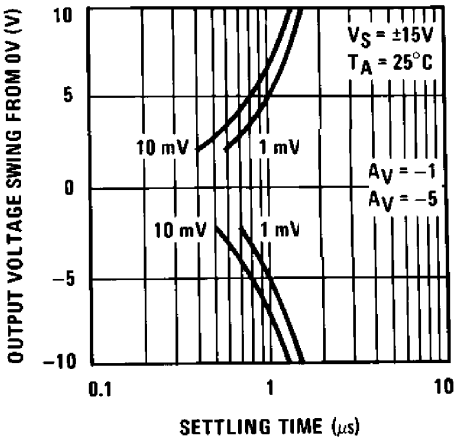

FIGURE 11. Inverter Settling Time

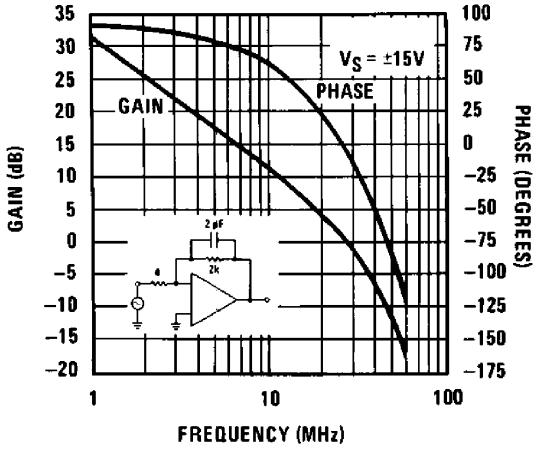

FIGURE 12. Bode Plot

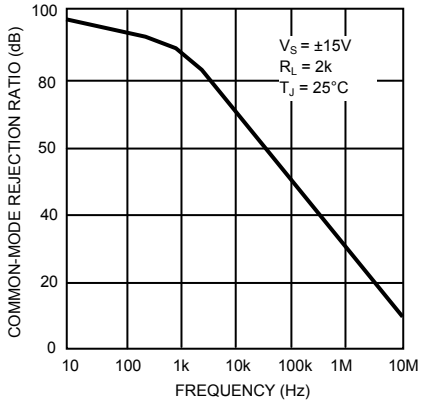

FIGURE 13. COMMON-MODE REJECTION RATIO