CMOS High Voltage Logic - MM74C906N

Hex Open Drain N-Channel Buffers in Plastic Dual-In-Line Package (PDIP)

Rev 1.0
16/07/2021

Description

The MM74C906N buffer employs monolithic CMOS technology in achieving open drain outputs. The MM74C906N consists of six inverters driving six N-channel devices. The open-drain feature of these buffers makes level shifting or wire-AND and wire-OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

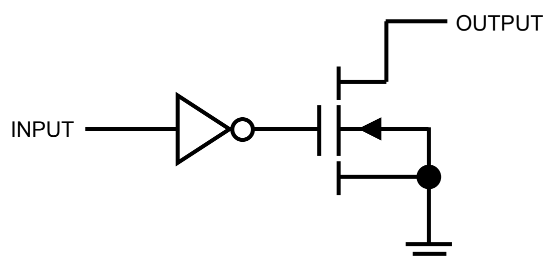
Features:

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- High current sourcing and sinking open-drain outputs

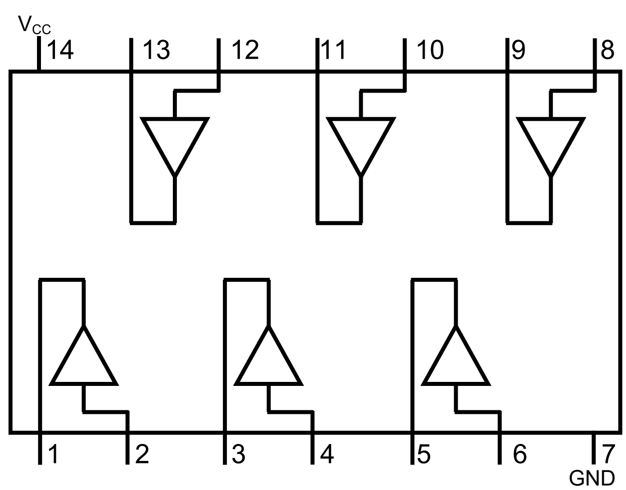
Ordering Information

The following part suffixes apply:

MM74C906N - 14 Lead Plastic Dual-In-Line Package



Schematic & Connection Diagram



Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
Voltage at any input pin	V_{IN}	-0.3 to V_{CC} + 0.3	V
Voltage at any output pin	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating V_{CC} range	V_{CC}	3 to 15	V
Absolute maximum V_{CC}	$V_{CC(MAX)}$	18	V
Maximum Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	260	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

DC Electrical Characteristics T_A = -40 to +85°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 5V	3.5	-	-	V
		V_{CC} = 10V	8.0	-	-	V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 5V	-	-	1.5	V
		V_{CC} = 10V	-	-	2.0	V
Logical "1" Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V	-	0.005	1	µA
Logical "0" Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V	-1.0	-0.005	-	µA
Supply Current	I_{CC}	V_{CC} = 15V,Output Open	-	0.05	15	µA
Output Leakage Current		V_{CC} = 4.75V, V_{IN} = V_{CC} – 1.5V, V_{CC}=4.75V,V_{OUT} =18V	-	0.005	5	µA
CMOS/LPTTL INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 4.75V	V_{CC} -1.5V	-	-	V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 4.75V	-	-	0.8	V
OUTPUT DRIVE CURRENT						
		V_{CC} = 4.75V, V_{IN} = 1V + 0.1 V_{CC}, V_{CC}=4.75V,V_{OUT} =0.5V	2.1	8.0	-	mA
		V_{CC} = 4.75V, V_{IN} = 1V + 0.1 V_{CC}, V_{CC}=4.75V,V_{OUT} =1.0V	4.2	12.0	-	mA
		V_{CC} = 10V, V_{IN} = 2V, V_{CC}= 10V,V_{OUT} =0.5V	4.2	20	-	mA
		V_{CC} = 10V, V_{IN} = 2V, V_{CC}= 10V,V_{OUT} =1V	8.4	30	-	mA

Dynamic Electrical Characteristics[2] T_A = 25°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "0"	t_{pd}	V_{CC} = 5.0V, R = 10kΩ, C_L = 50pF	-	-	150	ns
Propagation Delay Time to Logical "1"	t_{pd}	V_{CC} = 10V, R = 10kΩ, C_L = 50pF	-	-	75	ns
Input Capacitance	C_{IN}	-	-	5.0	-	pF
Output Capacitance	C_{OUT}	-	-	20	-	pF
Power Dissipation Capacitance[2]	C_{PD}	-	-	30	-	pF

2. Per Buffer, used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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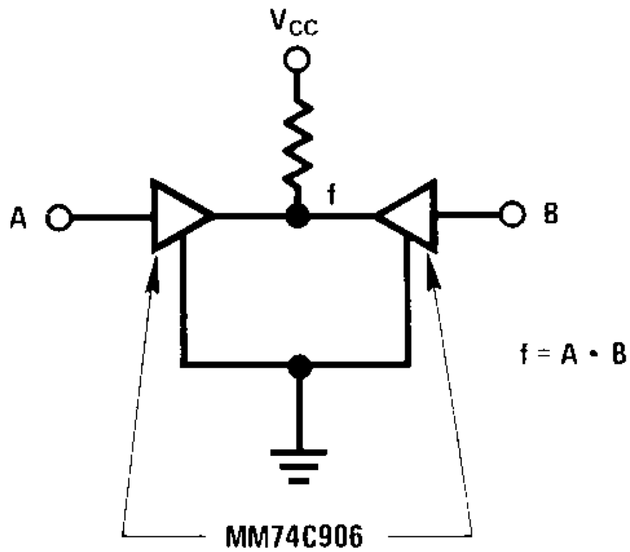
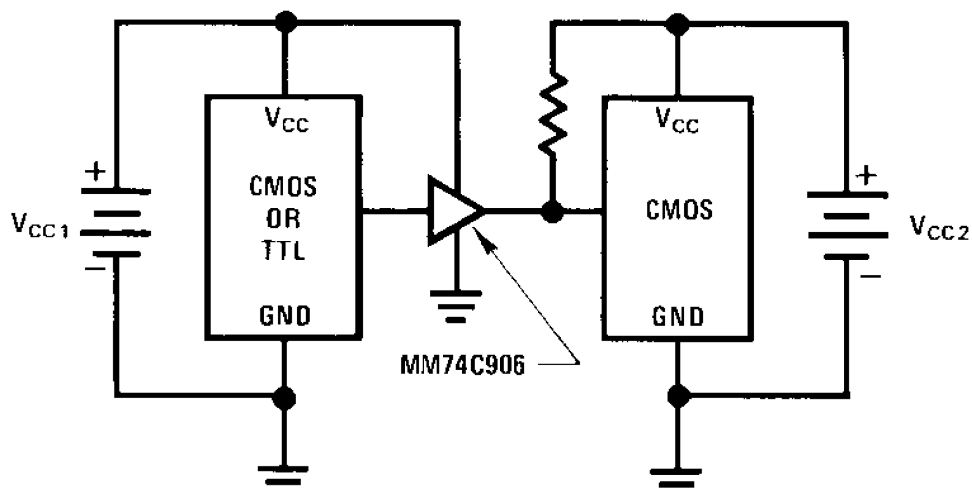
Typical Applications

Wire AND Gate



Note: Can be extended to more than 2 inputs

CMOS or TTL to CMOS at a Higher V_{CC}



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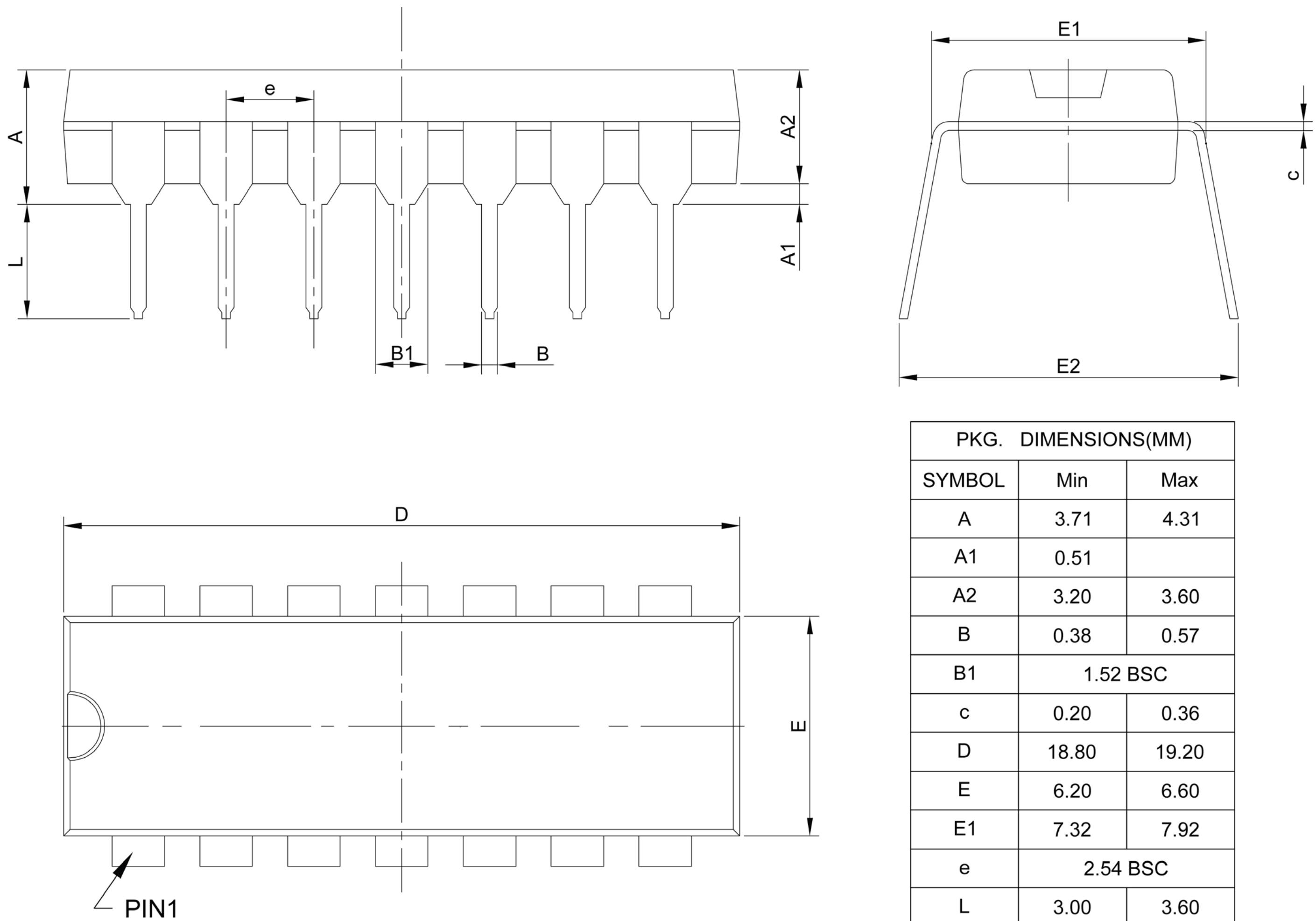
14 Lead Plastic DIP - Package Dimensions and Footprint



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	3.71	4.31
A1	0.51	
A2	3.20	3.60
B	0.38	0.57
B1	1.52 BSC	
c	0.20	0.36
D	18.80	19.20
E	6.20	6.60
E1	7.32	7.92
e	2.54 BSC	
L	3.00	3.60
E2	8.40	9.00