



# CMOS High Voltage Logic - MM74C906M

Hex Open Drain N-Channel Buffers in Plastic Small-Outline Package (SOIC)

Rev 1.0  
16/07/2021

## Description

The MM74C906M buffer employs monolithic CMOS technology in achieving open drain outputs. The MM74C906M consists of six inverters driving six N-channel devices. The open-drain feature of these buffers makes level shifting or wire-AND and wire-OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to  $V_{CC}$  and to ground.

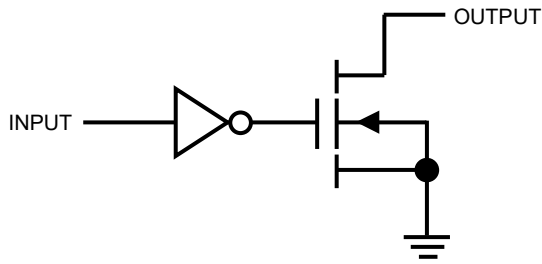
## Features:

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity:  $0.45 V_{CC}$  (typ.)
- High current sourcing and sinking open-drain outputs

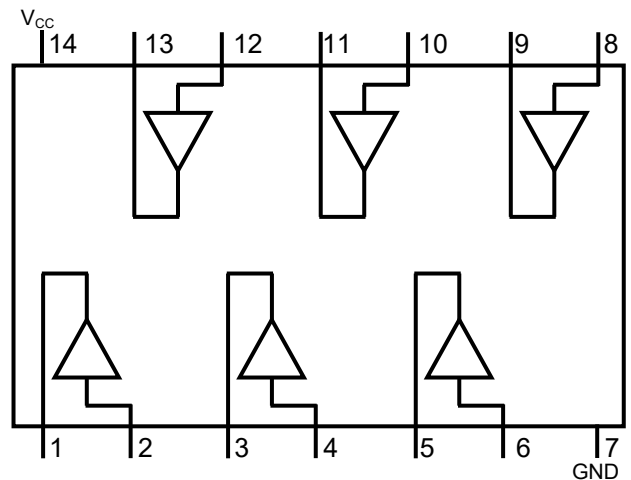
## Ordering Information

The following part suffixes apply:

**MM74C906M** - 14 Lead Plastic SOIC Package



## Schematic & Connection Diagram



## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
Voltage at any input pin	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	V
Voltage at any output pin	$V_{OUT}$	-0.3 to $V_{CC} + 0.3$	V
Operating $V_{CC}$ range	$V_{CC}$	3 to 15	V
Absolute maximum $V_{CC}$	$V_{CC(MAX)}$	18	V
Maximum Power Dissipation	$P_D$	700	mW
Operating Temperature Range	$T_A$	-40 to +85	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature (Soldering, 10 seconds)	$T_L$	260	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.





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## DC Electrical Characteristics $T_A = -40$ to $+85^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>CMOS TO CMOS</b>						
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC} = 5V$	3.5	-	-	V
		$V_{CC} = 10V$	8.0	-	-	V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC} = 5V$	-	-	1.5	V
		$V_{CC} = 10V$	-	-	2.0	V
Logical "1" Input Current	$I_{IN(1)}$	$V_{CC} = 15V, V_{IN} = 15V$	-	0.005	1	$\mu\text{A}$
Logical "0" Input Current	$I_{IN(0)}$	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005	-	$\mu\text{A}$
Supply Current	$I_{CC}$	$V_{CC} = 15V, \text{Output Open}$	-	0.05	15	$\mu\text{A}$
Output Leakage Current		$V_{CC} = 4.75V,$ $V_{IN} = V_{CC} - 1.5V,$ $V_{CC}=4.75V, V_{OUT} = 18V$	-	0.005	5	$\mu\text{A}$
<b>CMOS/LPTTL INTERFACE</b>						
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC} = 4.75V$	$V_{CC}$ -1.5V	-	-	V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC} = 4.75V$	-	-	0.8	V
<b>OUTPUT DRIVE CURRENT</b>						
		$V_{CC} = 4.75V,$ $V_{IN} = 1V + 0.1 V_{CC},$ $V_{CC}=4.75V, V_{OUT} = 0.5V$	2.1	8.0	-	mA
		$V_{CC} = 4.75V,$ $V_{IN} = 1V + 0.1 V_{CC},$ $V_{CC}=4.75V, V_{OUT} = 1.0V$	4.2	12.0	-	mA
		$V_{CC} = 10V, V_{IN} = 2V,$ $V_{CC}= 10V, V_{OUT} = 0.5V$	4.2	20	-	mA
		$V_{CC} = 10V, V_{IN} = 2V,$ $V_{CC}= 10V, V_{OUT} = 1V$	8.4	30	-	mA

## Dynamic Electrical Characteristics<sup>2</sup> $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "0"	$t_{pd}$	$V_{CC} = 5.0V,$ $R = 10k\Omega, C_L = 50pF$	-	-	150	ns
Propagation Delay Time to Logical "1"	$t_{pd}$	$V_{CC} = 10V,$ $R = 10k\Omega, C_L = 50pF$	-	-	75	ns
Input Capacitance	$C_{IN}$	-	-	5.0	-	pF
Output Capacitance	$C_{OUT}$	-	-	20	-	pF
Power Dissipation Capacitance <sup>2</sup>	$C_{PD}$	-	-	30	-	pF

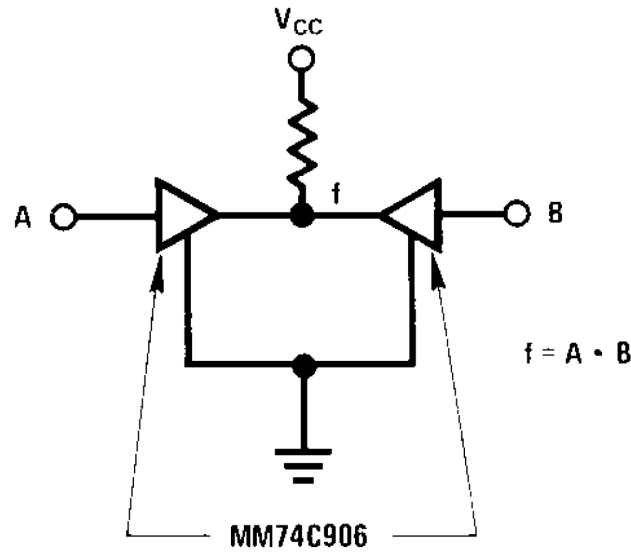
2. Per Buffer, used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .





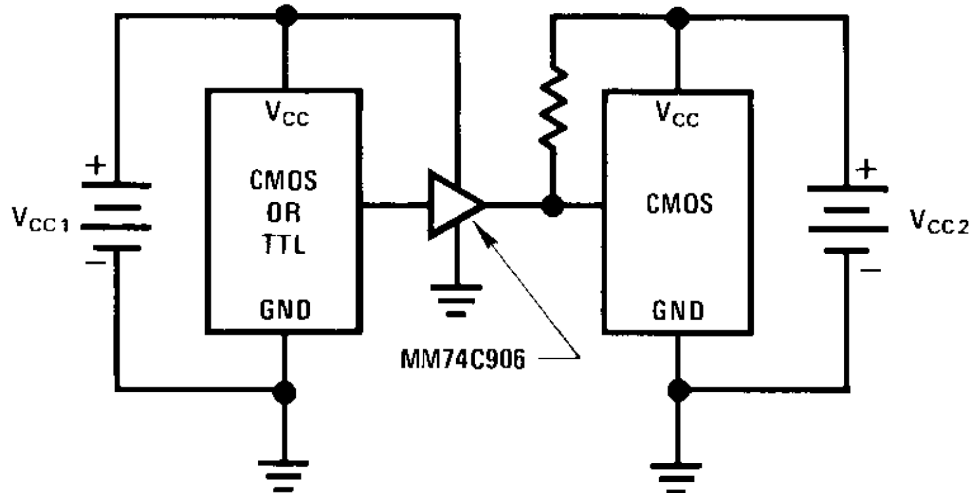
## Typical Applications

### Wire AND Gate



Note: Can be extended to more than 2 inputs

### CMOS or TTL to CMOS at a Higher $V_{CC}$

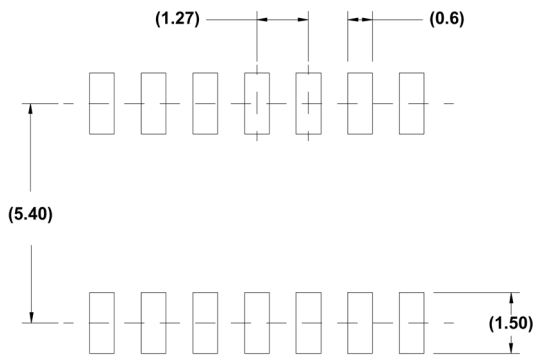
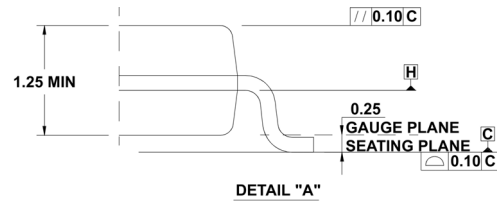
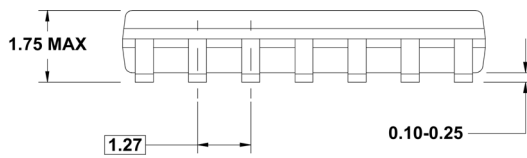
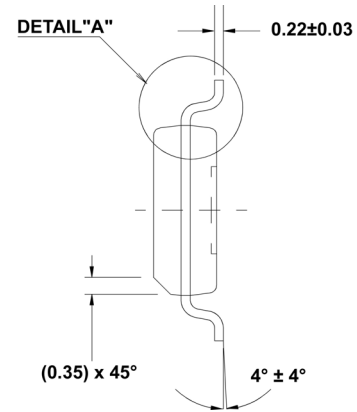
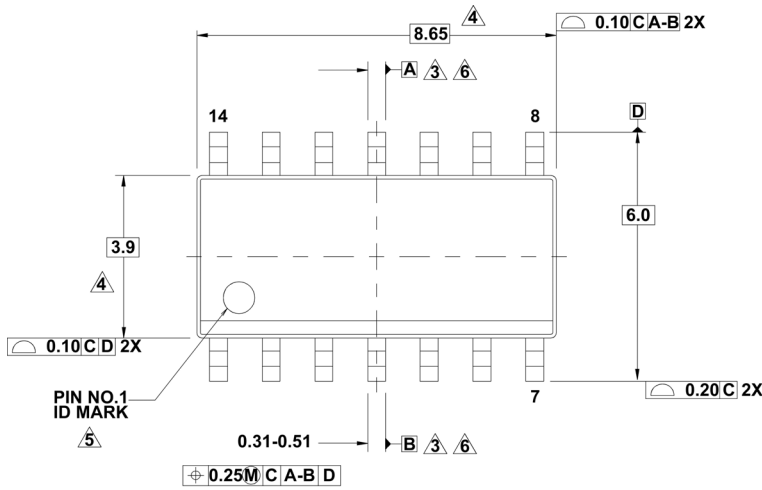




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## SOIC 14 - Package Dimensions and Footprint



### NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.  
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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