



CMOS High Voltage Logic – MM54C14J

Hex Schmitt Trigger Inverter in Ceramic Dual-In-Line Package (CDIP)

Rev 1.0
17/02/2023

Description

The MM54C14J Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-} , show low variation with respect to temperature (typ. $0.0005V/°C$ at $V_{CC} = 10V$), and hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{CC}$ is guaranteed. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide supply voltage range: 3V to 15V
- High noise immunity: $0.70 V_{CC}$ (typ.)
- Low power TTL compatibility:
 - $0.40 V_{CC}$ (typ.)
 - $0.20 V_{CC}$ (guaranteed)
- Hysteresis:
 - $0.40 V_{CC}$ (typ.)
 - $0.20 V_{CC}$ (guaranteed).

Ordering Information

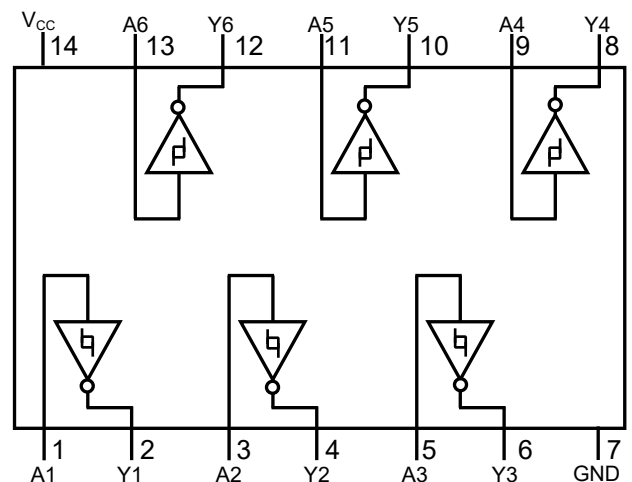
The following part suffixes apply:

MM54C14J - 14 Lead Ceramic Dual-In-Line Package

Function Table

INPUT A	OUTPUT Y
L	H
H	L

Schematic & Connection Diagram



Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
Voltage at any input pin	V_{IN}	-0.3 to $V_{CC} + 0.3$	V
Voltage at any output pin	V_{OUT}	-0.3 to $V_{CC} + 0.3$	V
Operating V_{CC} range	V_{CC}	3 to 15	V
Absolute maximum V_{CC}	$V_{CC(MAX)}$	18	V
Maximum Power Dissipation	P_D	700	mW
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	260	°C

¹ Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.





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DC Electrical Characteristics $T_A = -55$ to $+125^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Positive Going Threshold Voltage	V_{T+}	$V_{CC} = 5\text{V}$	3.0	3.6	4.3	V
		$V_{CC} = 10\text{V}$	6.0	6.8	8.6	V
		$V_{CC} = 15\text{V}$	9.0	10.0	12.9	V
Negative Going Threshold Voltage	V_{T-}	$V_{CC} = 5\text{V}$	0.7	1.4	2.0	V
		$V_{CC} = 10\text{V}$	1.4	3.2	4.0	V
		$V_{CC} = 15\text{V}$	2.1	5.0	6.0	V
Hysteresis	$V_{T+} - V_{T-}$	$V_{CC} = 5\text{V}$	1.0	2.2	3.6	V
		$V_{CC} = 10\text{V}$	2.0	3.6	7.2	V
		$V_{CC} = 15\text{V}$	3.0	5.0	10.8	V
Logical "1" Output Voltage	$V_{OUT(1)}$	$V_{CC} = 5\text{V}, I_O = -10\mu\text{A}$	4.5	-	-	V
		$V_{CC} = 10\text{V}, I_O = -10\mu\text{A}$	9.0	-	-	V
Logical "0" Output Voltage	$V_{OUT(0)}$	$V_{CC} = 5\text{V}, I_O = 10\mu\text{A}$	-	-	0.5	V
		$V_{CC} = 10\text{V}, I_O = 10\mu\text{A}$	-	-	1.0	V
Logical "1" Input Current	$I_{IN(1)}$	$V_{CC} = 15\text{V}, V_{IN} = 15\text{V}$	-	0.005	1.0	μA
Logical "0" Input Current	$I_{IN(0)}$	$V_{CC} = 15\text{V}, V_{IN} = 0\text{V}$	-1.0	-0.005	-	μA
Supply Current	I_{CC}	$V_{CC} = 15\text{V}, V_{IN} = 0\text{V}/15\text{V}$	-	0.05	15	μA
Supply Current ²	I_{CC}	$V_{CC} = 5\text{V}, V_{IN} = 2.5\text{V}$	-	20	-	μA
		$V_{CC} = 10\text{V}, V_{IN} = 5\text{V}$	-	200	-	μA
		$V_{CC} = 15\text{V}, V_{IN} = 7.5\text{V}$	-	600	-	μA
CMOS/LPTTL INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC} = 5\text{V}$	4.3	-	-	V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC} = 5\text{V}$	-	-	0.7	V
Logical "1" Output Voltage	$V_{OUT(1)}$	$V_{CC} = 4.5\text{V}, I_O = -360\mu\text{A}$	2.4	-	-	V
Logical "0" Output Voltage	$V_{OUT(0)}$	$V_{CC} = 4.5\text{V}, I_O = 360\mu\text{A}$	-	-	0.4	V
OUTPUT DRIVE CURRENT $T_A = 25^\circ\text{C}$						
Output Source Current (P-Channel)	I_{SOURCE}	$V_{CC} = 5\text{V}, V_{OUT} = 0\text{V}$	-1.75	-3.3	-	mA
		$V_{CC} = 10\text{V}, V_{OUT} = 0\text{V}$	-8.0	-15	-	mA
Output Source Current (N-Channel)	I_{SINK}	$V_{CC} = 5\text{V}, V_{OUT} = V_{CC}$	1.75	3.6	-	mA
		$V_{CC} = 10\text{V}, V_{OUT} = V_{CC}$	8.0	16	-	mA
DYNAMIC ELECTRICAL CHARACTERISTICS³ $T_A = 25^\circ\text{C}, C_L = 50\text{pF}$ unless otherwise stated						
Propagation Delay from Input to Output	t_{PD0}, t_{PD1}	$V_{CC} = 5\text{V}$	-	220	400	ns
		$V_{CC} = 10\text{V}$	-	80	200	ns
Input Capacitance	C_{IN}	Any Input	-	5.0	-	pF
Power Dissipation Capacitance ⁴	C_{PD}	Per Gate	-	20	-	pF

2. Only one of the six inputs is at $\frac{1}{2} V_{CC}$; the others are either at V_{CC} or GND. 3. Not production tested in die form, characterized by chip design.

4. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.





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Typical Characteristics

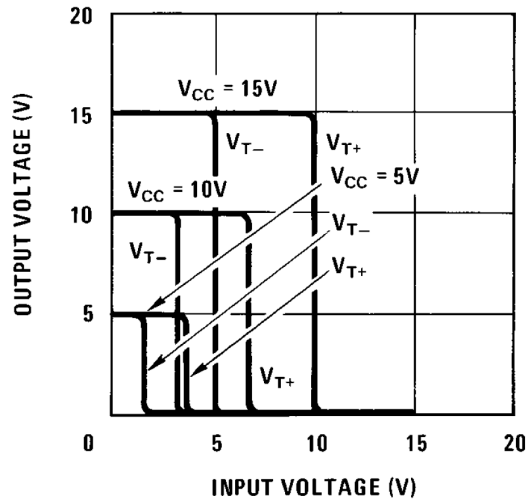


Figure 1 – Transfer Characteristics

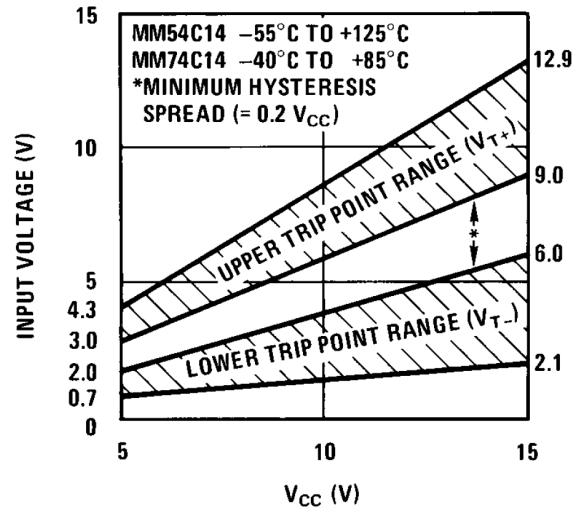


Figure 2 – Guaranteed Trip Point Range

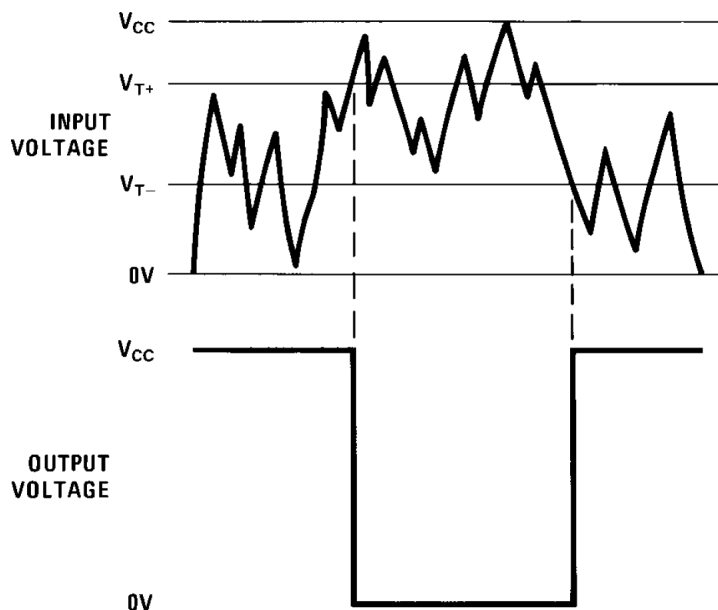


Figure 3 – Waveform



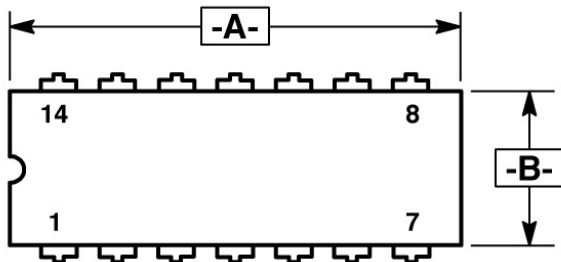
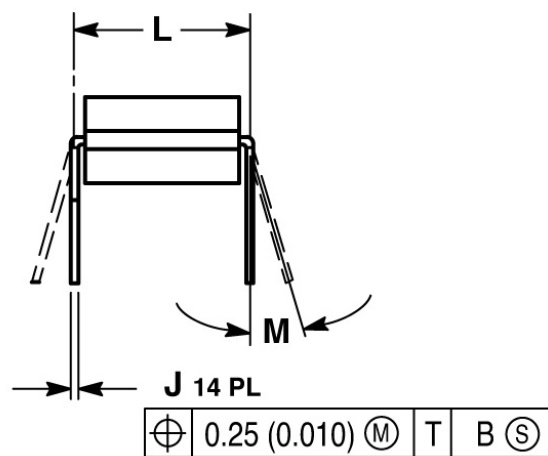
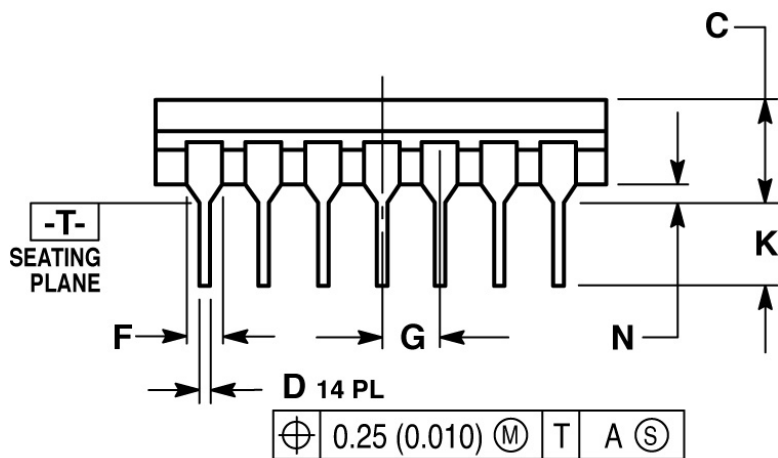


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14 Lead Ceramic DIP - Package Dimensions and Footprint



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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