# CMOS High Voltage Logic – MM54C14

**Hex Schmitt Trigger Inverter in bare die form**

**Rev 1.0**
**17/02/2023**

## Description

The MM54C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The positive and negative going threshold voltages, $V_{T+}$ and $V_{T-}$, show low variation with respect to temperature (typ. 0.0005V/°C at $V_{CC}$ = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2$ $V_{CC}$ is guaranteed. All inputs are protected from damage due to static discharge by diode clamps to $V_{CC}$ and GND.

## Features:

- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.70 $V_{CC}$ (typ.)
- Low power TTL compatibility:
  - o 0.40 $V_{CC}$ (typ.)
  - o 0.20 $V_{CC}$ (guaranteed)
- Hysteresis:
  - o 0.40 $V_{CC}$ (typ.)
  - o 0.20 $V_{CC}$ (guaranteed).

## Ordering Information

The following part suffixes apply:

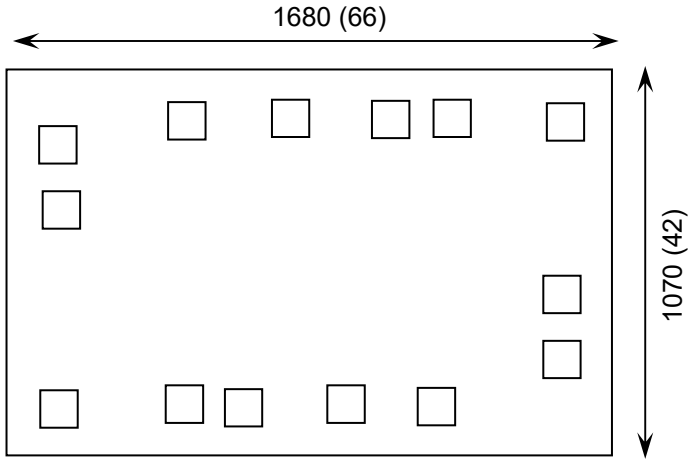
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

## Die Dimensions in µm (mils)




## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

| | | |
|---|---|---|
| Die Size (Unsawn) | 1680 x 1070<br>66.14 x 42.13 | µm<br>mils |
| Minimum Bond Pad Size | 105 x 105<br>4.713 x 4.13 | µm<br>mils |
| Die Thickness | 350 (±20)<br>13.78 (±0.79) | µm<br>mils |
| Top Metal Composition | Al 1%Si 1.1µm | |
| Back Metal Composition | N/A – Bare Si | |

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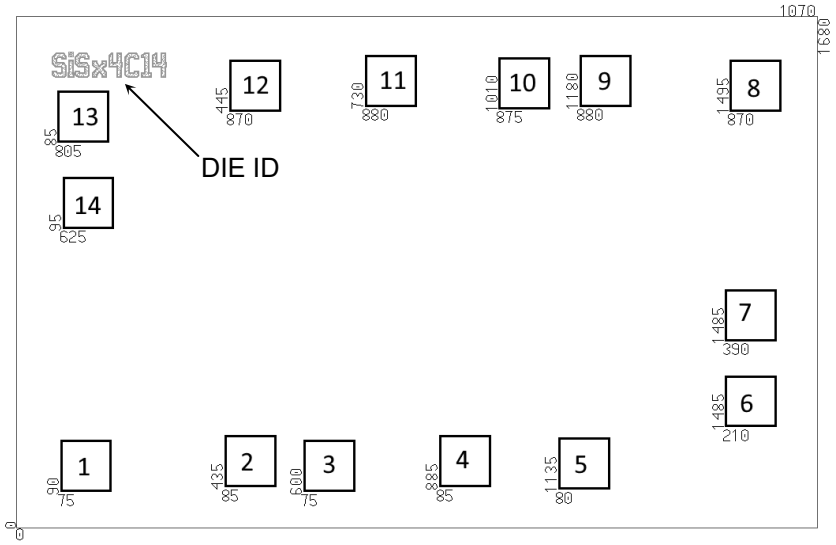
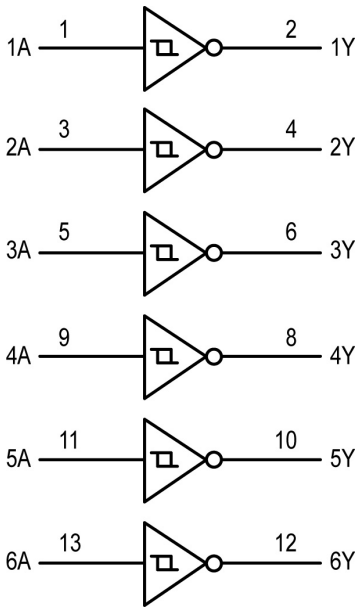
## Pad Layout and Functions




| PAD | FUNCTION | COORDINATES (µm) | |
|---|---|---|---|
| | | X | Y |
| 1 | 1A | 90 | 75 |
| 2 | 1Y | 435 | 85 |
| 3 | 2A | 600 | 75 |
| 4 | 2Y | 885 | 85 |
| 5 | 3A | 1135 | 80 |
| 6 | 3Y | 1485 | 210 |
| 7 | GND | 1485 | 390 |
| 8 | 4Y | 1495 | 870 |
| 9 | 4A | 1180 | 880 |
| 10 | 5Y | 1010 | 875 |
| 11 | 5A | 730 | 880 |
| 12 | 6Y | 445 | 870 |
| 13 | 6A | 85 | 805 |
| 14 | $V_{CC}$ | 95 | 625 |
| CONNECT CHIP BACK TO $V_{CC}$ | | | |

## Logic Diagram




Pad 14 = $V_{CC}$
Pad 7 = GND

## Function Table

| INPUT A | OUTPUT Y |
|---|---|
| L | H |
| H | L |

## Absolute Maximum Ratings[1]

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Voltage at any input pin | $V_{IN}$ | -0.3 to $V_{CC}$ + 0.3 | V |
| Voltage at any output pin | $V_{OUT}$ | -0.3 to $V_{CC}$ + 0.3 | V |
| Operating $V_{CC}$ range | $V_{CC}$ | 3 to 15 | V |
| Absolute maximum $V_{CC}$ | $V_{CC(MAX)}$ | 18 | V |
| Maximum Power Dissipation[2] | $P_D$ | 700 | mW |
| Operating Temperature Range | $T_A$ | -55 to +125 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | °C |

**1.** Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## DC Electrical Characteristics $T_A$ = -55 to +125°C unless otherwise stated

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| Positive Going Threshold Voltage | $V_{T+}$ | $V_{CC}$ = 5V | 3.0 | 3.6 | 4.3 | V |
| | | $V_{CC}$ = 10V | 6.0 | 6.8 | 8.6 | V |
| | | $V_{CC}$ = 15V | 9.0 | 10.0 | 12.9 | V |
| Negative Going Threshold Voltage | $V_{T-}$ | $V_{CC}$ = 5V | 0.7 | 1.4 | 2.0 | V |
| | | $V_{CC}$ = 10V | 1.4 | 3.2 | 4.0 | V |
| | | $V_{CC}$ = 15V | 2.1 | 5.0 | 6.0 | V |
| Hysteresis | $V_{T+} - V_{T-}$ | $V_{CC}$ = 5V | 1.0 | 2.2 | 3.6 | V |
| | | $V_{CC}$ = 10V | 2.0 | 3.6 | 7.2 | V |
| | | $V_{CC}$ = 15V | 3.0 | 5.0 | 10.8 | V |
| Logical “1” Output Voltage | $V_{OUT(1)}$ | $V_{CC}$ = 5V, $I_O$ = -10µA | 4.5 | - | - | V |
| | | $V_{CC}$ = 10V, $I_O$ = -10µA | 9.0 | - | - | V |
| Logical “0” Output Voltage | $V_{OUT(0)}$ | $V_{CC}$ = 5V, $I_O$ = 10µA | - | - | 0.5 | V |
| | | $V_{CC}$ = 10V, $I_O$ = 10µA | - | - | 1.0 | V |
| Logical “1” Input Current | $I_{IN(1)}$ | $V_{CC}$ = 15V, $V_{IN}$ = 15V | - | 0.005 | 1.0 | µA |
| Logical “0” Input Current | $I_{IN(0)}$ | $V_{CC}$ = 15V, $V_{IN}$ = 0V | -1.0 | -0.005 | - | µA |
| Supply Current | $I_{CC}$ | $V_{CC}$ =15V,$V_{IN}$=0V/15V | - | 0.05 | 15 | µA |
| Supply Current[3] | $I_{CC}$ | $V_{CC}$ = 5V, $V_{IN}$ = 2.5V | - | 20 | - | µA |
| | | $V_{CC}$ = 10V, $V_{IN}$ = 5V | - | 200 | - | µA |
| | | $V_{CC}$ = 15V, $V_{IN}$ = 7.5V | - | 600 | - | µA |

**3.** Only one of the six inputs is at ½ $V_{CC}$; the others are either at $V_{CC}$ or GND.

## DC Electrical Characteristics $T_A$ = -55 to +125°C unless otherwise stated

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CMOS/LPTTL INTERFACE** | | | | | | |
| Logical "1" Input Voltage | $V_{IN(1)}$ | $V_{CC}$ = 5V | 4.3 | - | - | V |
| Logical "0" Input Voltage | $V_{IN(0)}$ | $V_{CC}$ = 5V | - | - | 0.7 | V |
| Logical "1" Output Voltage | $V_{OUT(1)}$ | $V_{CC}$= 4.5V,$I_O$= -360µA | 2.4 | - | - | V |
| Logical "0" Output Voltage | $V_{OUT(0)}$ | $V_{CC}$ =4.5V, $I_O$ = 360µA | - | - | 0.4 | V |
| **OUTPUT DRIVE CURRENT $T_A$ = 25°C** | | | | | | |
| Output Source Current (P-Channel) | $I_{SOURCE}$ | $V_{CC}$ = 5V, $V_{OUT}$ = 0V | -1.75 | -3.3 | - | mA |
| | | $V_{CC}$ = 10V, $V_{OUT}$ = 0V | -8.0 | -15 | - | mA |
| Output Source Current (N-Channel) | $I_{SINK}$ | $V_{CC}$ = 5V, $V_{OUT}$ = $V_{CC}$ | 1.75 | 3.6 | - | mA |
| | | $V_{CC}$ = 10V, $V_{OUT}$ = $V_{CC}$ | 8.0 | 16 | - | mA |
| **DYNAMIC ELECTRICAL CHARACTERISTICS[4] $T_A$ = 25°C, $C_L$ = 50pF unless otherwise stated** | | | | | | |
| Propagation Delay from Input to Output | $t_{PD0}$, $t_{PD1}$ | $V_{CC}$ = 5V | - | 220 | 400 | ns |
| | | $V_{CC}$ = 10V | - | 80 | 200 | ns |
| Input Capacitance | $C_{IN}$ | Any Input | - | 5.0 | - | pF |
| Power Dissipation Capacitance[5] | $C_{PD}$ | Per Gate | - | 20 | - | pF |

**4.** Not production tested in die form, characterized by chip design.
**5.** Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

## Typical Characteristics

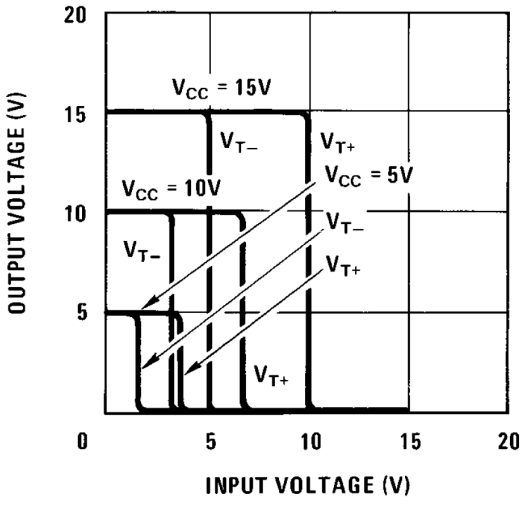



**Figure 1** – Transfer Characteristics

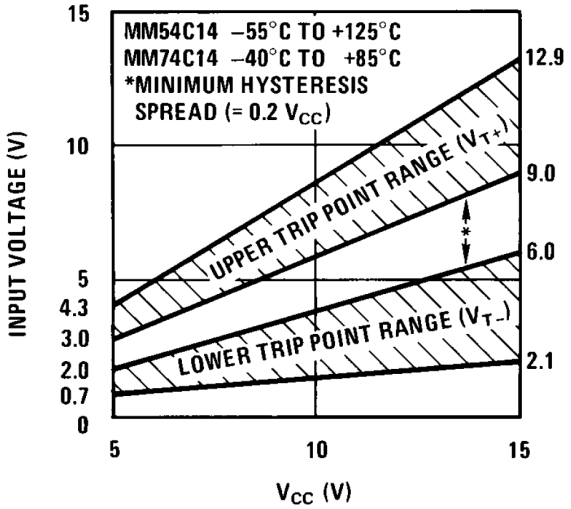



**Figure 2** – Guaranteed Trip Point Range

## Typical Characteristics continued

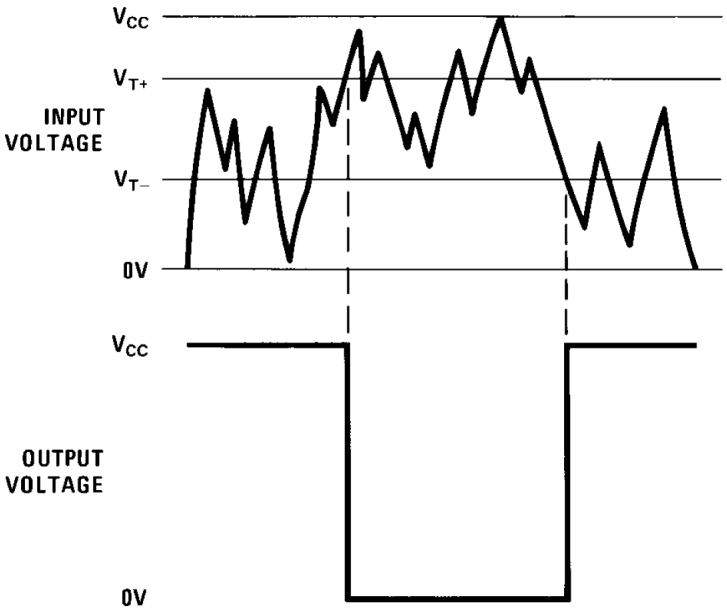



**Figure 3** – Waveform