CMOS Low Power Timer – LMC555

Precision Timing Generator / Oscillator in bare die form

Rev 1.1
21/01/18

Description

The LMC555 is a highly stable timer for use in precision timing and oscillator applications. As timer (monostable), the device is capable of producing accurate time delays from microseconds through hours using x1 capacitor and x1 resistor. As oscillator (astable), the device can maintain an accurately controlled free running frequency + duty cycle with x2 external resistors and x1 capacitor. The LMC555 may be triggered by the falling edge of the waveform signal. Device output can source or sink up to 200mA current and drive TTL/CMOS circuits. The LMC555 is a CMOS upgraded version of the popular bipolar 555 timer series and is drop-in compatible for most legacy 555 applications. The device also directly replaces TLC555 and ICM7555.

Features:

- Wide supply voltage range 2-18V
- Low Supply Current - 200µA max @ 2V
- High speed operation – Min 500kHz guaranteed
- Operates in both astable and monostable modes
- Adjustable Duty Cycle
- Output drives TTL/CMOS/MOS at 5V

For compatibility and improvements versus LM555, NE555, SE555, MC1455 and MC1555 products please see application notes.

Ordering Information

The following part suffixes apply:

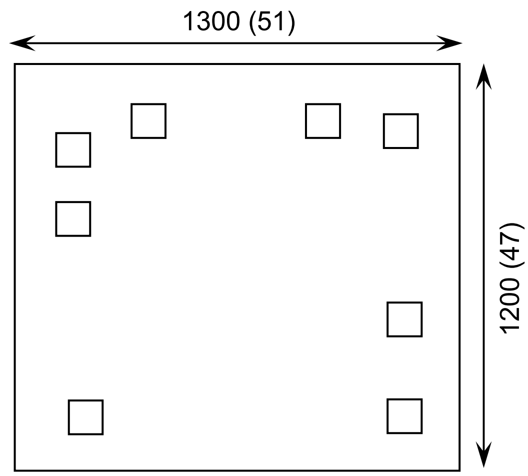
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



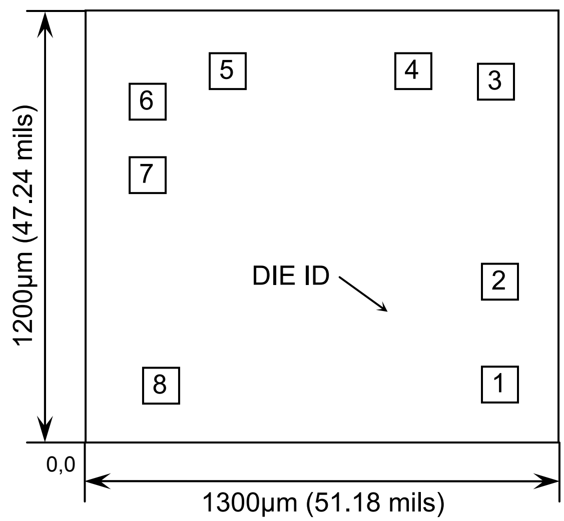
Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(15 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1300 x 1200 51 x 47	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	GND	1.084	0.119
2	$\overline{\text{TRIGGER}}$	1.084	0.4015
3	OUTPUT	1.0735	0.9545
4	$\overline{\text{RESET}}$	0.845	0.984
5	CONTROL VOLTAGE	0.3335	0.984
6	THRESHOLD	0.116	0.8995
7	DISCHARGE	0.116	0.6965
8	V_{DD}	0.1535	0.116
CHIP BACK POTENTIAL IS GND OR FLOAT			

Truth Table

THRESHOLD	$\overline{\text{TRIGGER}}$	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE
X	X	L	L	ON
> $2/3 \cdot V_{DD}$	> $1/3 \cdot V_{DD}$	H	L	ON
< $2/3 \cdot V_{DD}$	> $1/3 \cdot V_{DD}$	H	STABLE	STABLE
X	< $1/3 \cdot V_{DD}$	H	H	OFF

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD}	18	V
Output Current	I_O	100	mA
Input Voltage	V_{TH}, V_{TRIG}, V_{RESET}, V_{CTRL}	V_{DD} ±0.3	V
Operating Temperature Range	T_J	-55 to 125	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Power Dissipation in Still Air[2]	P_D	300	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic package at 25°C, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Supply Voltage	V_{DD}	2	18	V
Output Current	I_O	-	20	mA
Input Voltage	V_{TH}, V_{TRIG}, V_{RESET}	-0.3	V_{DD} +0.3	V

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Threshold Voltage	V_{TH}	5V	T_J = 25°C	3.25	3.35	3.50	V
			T_J = -55°C to +125°C	3	-	0.80	
Trigger Voltage	V_{TRIG}	5V	T_J = 25°C	1.55	1.65	1.80	V
			T_J = -55°C to +125°C	1.40	-	2.00	
Reset Voltage	V_{RESET}	2V 18V	T_J = 25°C	0.4	0.7	1	V
		2V 18V	T_J = -55°C to +125°C	0.2	-	1.5	
Control Voltage	V_{CTRL}	5V	T_J = 25°C	2.9	3.3	3.8	V
			T_J = -55°C to +125°C	-	-	-	
Low-Level Output Voltage	V_{OL}	5V	I_{OL} = 3.2mA, T_J = 25°C	-	-	0.40	V
		15V	I_{OL} = 20mA, T_J = 25°C	-	-	1.00	
		5V	I_{OL} = 3.2mA, T_J = 125°C	-	-	0.60	
		15V	I_{OL} = 20mA, T_J = 125°C	-	-	1.50	
High-Level Output Voltage	V_{OH}	5V	I_{OH} = -0.8mA, T_J = 25°C	4.00	-	-	V
		15V		14.30	-	-	
		5V	I_{OH} = -0.8mA, T_J = -55°C to +125°C	3.50	-	-	
		15V		14.00	-	-	
Supply Current[2]	I_{CC}	2V	T_J = 25°C	-	-	200	µA
		18V		-	-	300	
		2V	T_J = -55°C to +125°C	-	-	600	
		18V		-	-	1000	

2. Essentially independent of V_{TH}, V_{TRIG}, V_{RESET} voltages.

AC Electrical Characteristics[3]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Rise/Fall output time (Figure 1)	t_{THL}, t_{TLH}	5V	R_L = 10MΩ, C_L = 10pF T_J = 25°C	35	-	75	ns
			R_L = 10MΩ, C_L = 1pF T_J = -55°C to +125°C	70	-	150	
Guaranteed O_{SC} freq Astable operation	f_{MIN}	2-18V	T_J = 25°C	500	-	-	kHz
			T_J = -55°C to +125°C	200	-	-	
Initial Accuracy Error	-	-	-	-	-	5	%
Drift with Temperature	αf	5V	R_L = 1-100kΩ C_L = 0.1µF T_J = -55°C to +125°C	-	-	0.02	%/°C
		10V		-	-	0.03	
		15V		-	-	0.06	
Drift with Supply Voltage	Δf	5V	T_J = 25°C	-	-	3	%/B
			T_J = -55°C to +125°C			6	

3. Not production tested in die form, characterized by chip design and tested in package LAT.

Application Notes

The LMC555 is in most instances a direct replacement for the NE555, SE555 and LM555. Produced using a CMOS process this device offers the possibility to reduce the external passive component count and also delivers improved electrical performance. All unused inputs must be tied to an appropriate logic level to prevent false triggering.

Supply decoupling capacitor

All legacy bipolar 555 devices produce large crowbar currents in the output driver necessitating power supply decoupling via an external capacitor located close to the device. The LMC555 produces supply current spikes of only 2-3mA instead of 300-400mA, therefore supply decoupling is not normally necessary and optional.

Control Voltage decoupling capacitors

For most applications capacitors are not required and optional since the input impedance of the CMOS comparators is very high versus the legacy bipolar 555.

Supply Current

The supply current consumed by LMC555 is very low versus legacy 555. However, total system supply will be high unless the timing components are high impedance. Therefore, use high values for R and low values for C.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more the LMC555 will drive at least x2 standard TTL loads.

Application Notes Continued

Astable Mode

The circuit can be connected to trigger itself & free-run as a multivibrator (Figure 3). The output swings from rail-to-rail and is a true 50% duty cycle square wave. Less than a 1% frequency variation is observed over a voltage range of +5V to +15V. Duty Cycle is configurable by setting the ratio of resistors $R_A + R_B$ (Figure 4), the external capacitor charges through $R_A + R_B$ and discharges through R_B.

Monostable Mode

The timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2 the internal flip-flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t=R_AC$. When the voltage across the capacitor equals 2/3 V_{DD}, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly & drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state (Figure 2).

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltages as the standard bipolar 555 i.e. 0.6V to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the legacy bipolar 555 devices. If $\overline{\text{RESET}}$ is not used tie to V_{DD}.

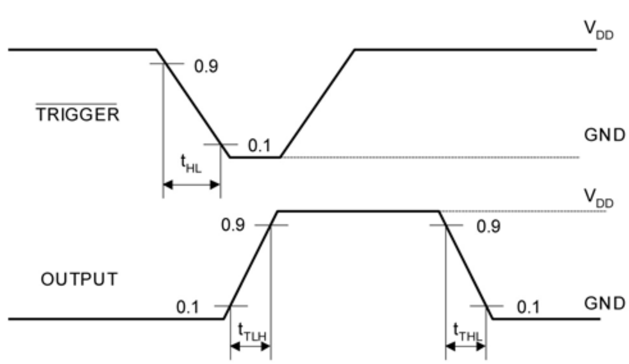


Figure 1 – Switching Waveform

Application Notes Continued

t_{OUTPUT} = -IN (1/3) R_AC = 1.1R_AC

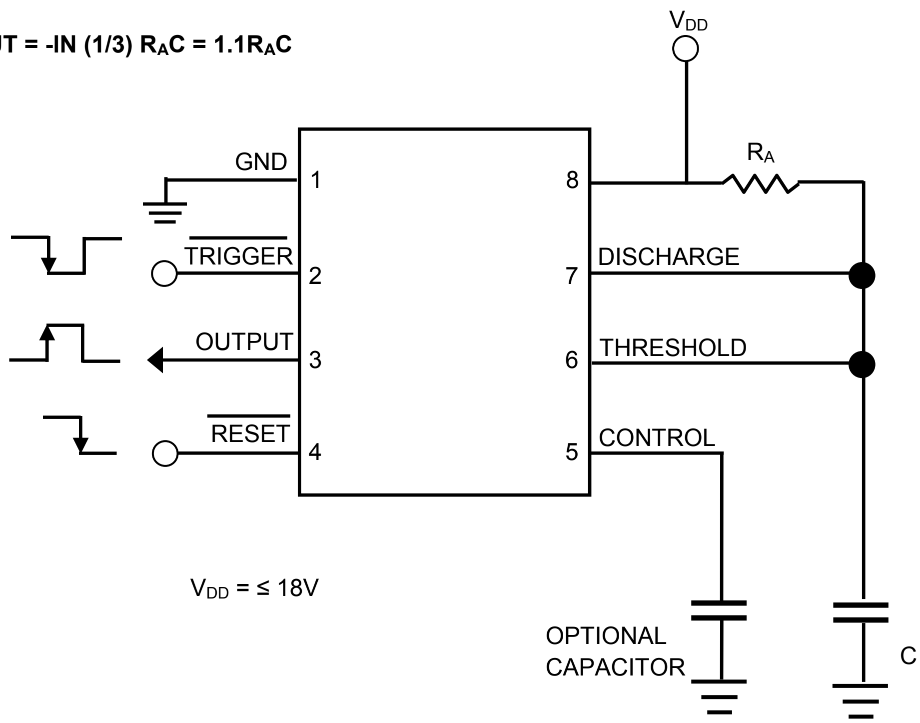


Figure 2 – Monostable Operation

$f = \frac{1}{1.4RC}$

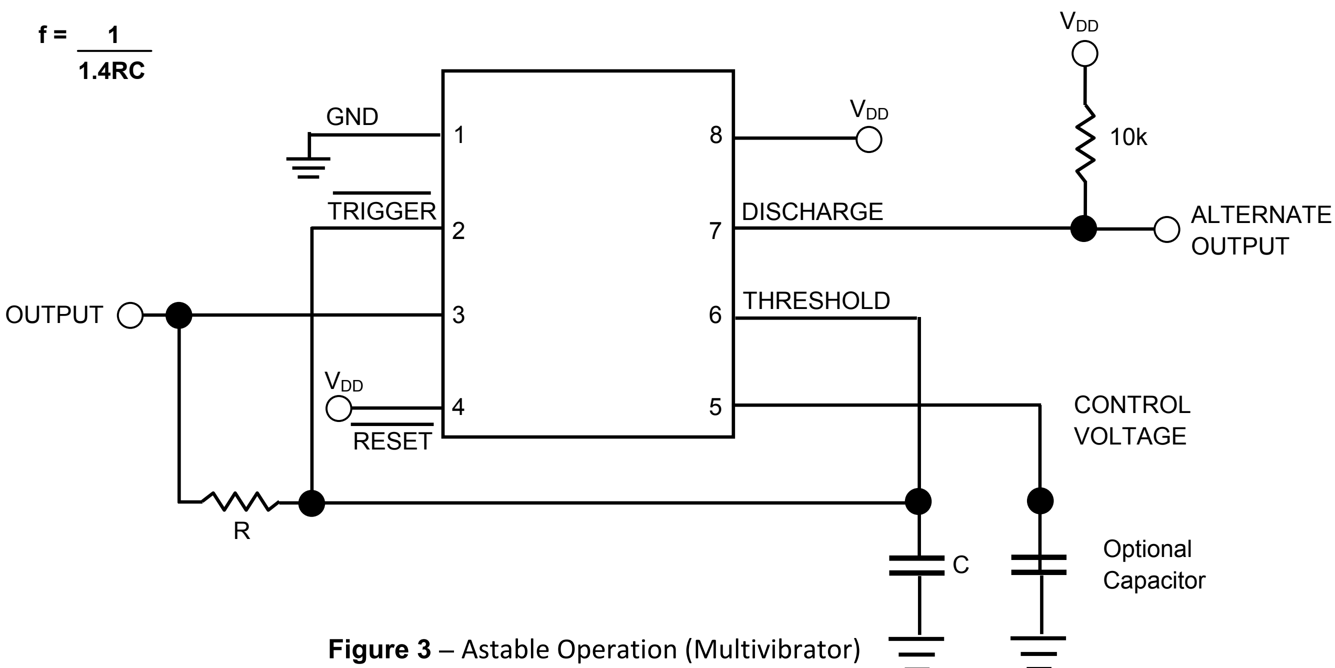


Figure 3 – Astable Operation (Multivibrator)

Application Notes Continued

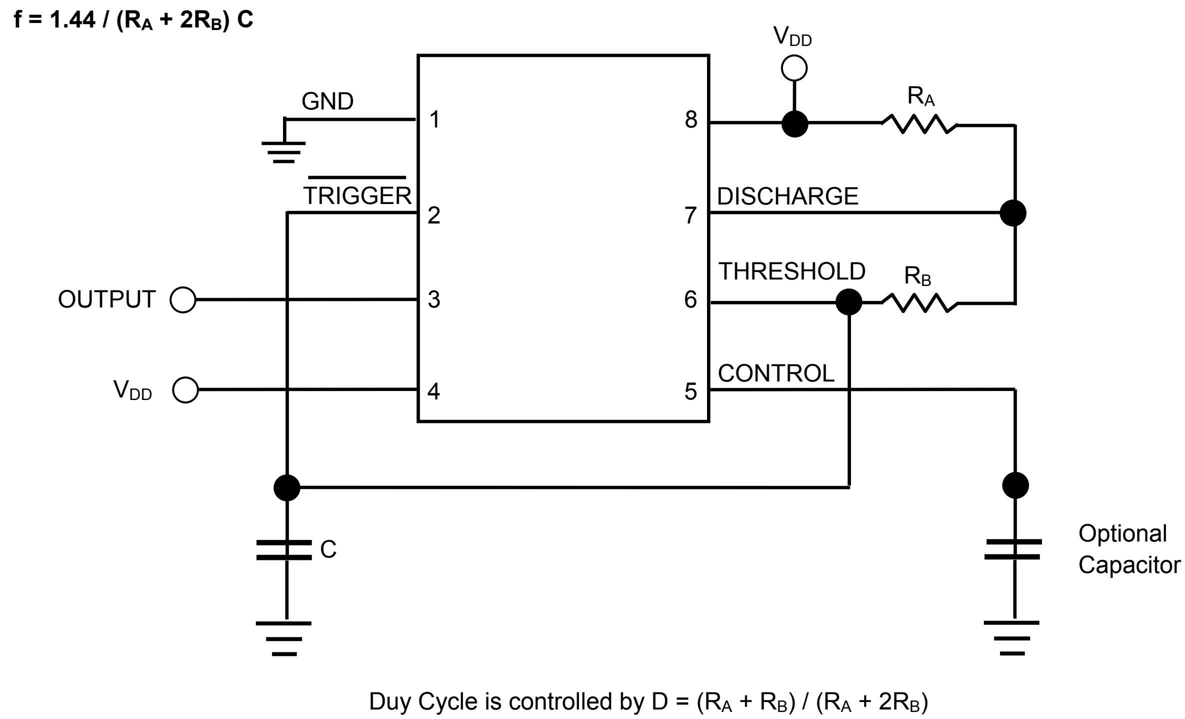


Figure 4 – Astable Operation (Adjustable Duty Cyle)

Application Notes Continued

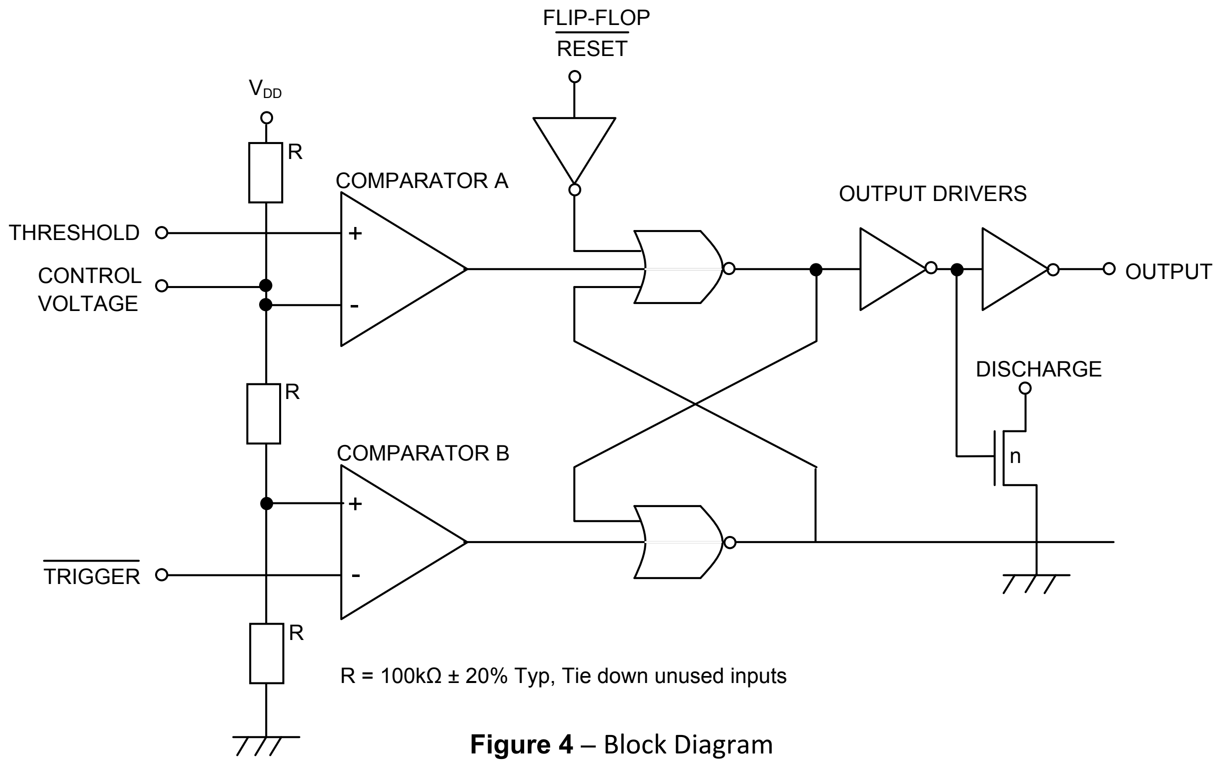


Figure 4 – Block Diagram