Linear Voltage Regulator – LM137

Negative adjustable 1.5A output Voltage Regulator in bare die form

Rev 1.1
30/05/19

Description

The LM137 is a high voltage adjustable 3-terminal voltage regulator with guaranteed 1.5A output current and equipped with internal limiting + thermal shutdown features for overload immunity. Output voltage is set by two external resistors. Additional to standard regulator function, the device can be used as a simple adjustable switching regulator; a programmable output regulator; or by connecting a fixed resistor between adjustment pin and output, can be used as a precision current regulator. A shutdown mechanism can be introduced by clamping the adjust terminal to ground which programs output to -1.2V where most loads draw little current.

Features:

- High temperature operation
- Output current in excess of 1.5A
- Adjustable output between -1.2V to -37V
- Internal short-circuit current limit
- Internal thermal overload protection
- Output transistor Safe-Area Compensation
- Floating operation for high voltage applications
- Typical 0.01% line, 0.3% load regulation
- Positive Voltage complement is LM117

Ordering Information

The following part suffixes apply:

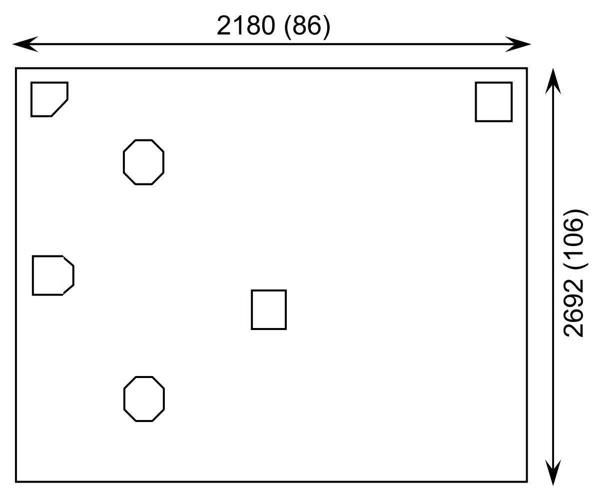
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

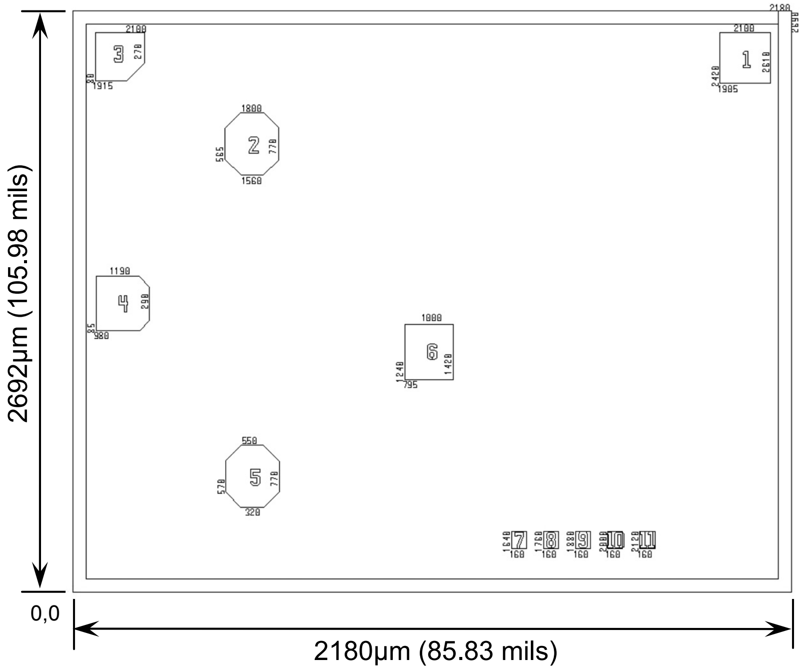
- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Tape & Reel – On request
- In Metal or Ceramic package – On request

Mechanical Specification

Die Size (Unsawn)	2180 x 2692 86 x 106	µm mils
Minimum Bond Pad Size	195 x 195 7.68 x 7.68	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 2.2µm	
Back Metal Composition	Ti/Ni/Ag 0.1-0.5-0.6µm	

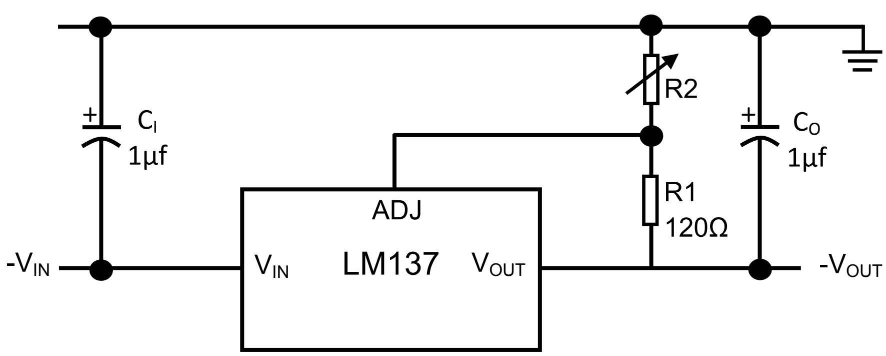
Rev 1.1
30/05/19

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	ADJ	2420	1905
2	V_{IN}	565	1560
3	V_{OUT}	80	1915
4	V_{OUT}	85	980
5	V_{IN}	570	320
6	V_{OUT}	1240	795
7	NC	1670	160
8	NC	1760	160
9	NC	1880	160
10	NC	2000	160
11	NC	2120	160
CONNECT CHIP BACK TO V_{IN}			

Typical Application



1.2V – 37V Adjustable Regulator

$$-V_{OUT} = -1.25V \left(1 + \frac{R2}{120\Omega}\right) + [-I_{ADJ}(R2)]$$

I_{ADJ} tolerance <100µA

C_I is required if the regulator is located an appreciable distance from power supply filter. C_O is required for stability. For optimum stability and transient response locate C_I C_O as close as possible to the regulator.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
Input–Output Voltage differential	V_{IN} - V_{OUT}	-40	V
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 to 150	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT
Output Voltage	V_{OUT}	-1.2	-37	V
Input–Output Voltage differential	V_{IN} - V_{OUT}	-4	-40	V
Output Current	I_{OUT}	0.01	1.5	A
Operating Junction Temperature Range	T_J	-55 to 150		°C

DC Electrical Characteristics V_{IN}-V_{OUT} = 5V, I_{OUT} = 0.5A, -55°C ≤ T_J +150°C, P_D ≤ 20W, I_{MAX} = 1.5A (unless noted otherwise)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	3V≤ |V_{IN} -V_{OUT}| ≤ 40V, 10mA ≤ I_{OUT} ≤ I_{MAX}	T_J =25°C	-1.225	-1.250	-1.275	V
			T_J =150°C	-1.200	-1.250	-1.300	
Line Regulation[2]	ΔV_{OUT}	3V≤ |V_{IN} - V_{OUT}| ≤ 40V, I_L = 10mA	T_J = 25°C	-	0.01	0.02	% / V_{OUT}
			T_J =150°C	-	0.02	0.05	
Load Regulation	ΔV_{OUT}	10mA ≤ I_{OUT} ≤ I_{MAX}	T_J = 25°C	-	0.3	0.5	%
			T_J =150°C	-	0.3	1	
Thermal Regulation	-	10ms pulse, T_J = 25°C		-	0.002	0.02	% / W
Adjustment Pin Current	I_{ADJ}			-	65	100	µA
Adjustment Pin Current Change	ΔI_{ADJ}	3V ≤ |V_{IN} - V_{OUT}| ≤ 40V, 10mA ≤ I_L ≤ I_{MAX}	T_J = 25°C	-	2	5	µA
Temperature Stability	-	T_{LOW} ≤ T_J ≤ T_{HIGH}		-	0.6	-	%
Minimum Load Current	I_L	|V_{IN} – V_{OUT}| ≤ 40V		-	2.5	5	mA
		|V_{IN} – V_{OUT}| ≤ 10V		-	1.2	3	
Output Current Limit	I_{MAX}	|V_{IN} – V_{OUT}| ≤ 15V		1.5	2.2	3.5	A
		|V_{IN} – V_{OUT}| = 40V		0.24	0.40	-	

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

2. Load and line regulation are specified at constant junction temperature. Change in V_O because of heating effects is covered under thermal regulation specification. Pulse testing with a low duty cycle is used.

Rev 1.1
30/05/19

DC Electrical Characteristics V_{IN}-V_{OUT} = 5V, I_{OUT} = 0.5A, -55°C ≤ T_J +150°C, P_D ≤ 20W, I_{MAX} = 1.5A (unless noted otherwise)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
RMS Output Noise, % of V_{OUT}	eN	10 Hz ≤ f ≤ 10 kHz	T_J = 25°C	-	0.003	-	%
Ripple Rejection Ratio	RR	V_{OUT} = -10V, f =120 Hz	C_{ADJ} 0μF	-	60	-	dB
			C_{ADJ} 10μF	66	77	-	
Long Term Stability	-	T_A = 125°C, 1000 hrs		-	0.3	1	%
Thermal Resistance[3]	$R\theta_{JC}$	T_{LOW} ≤ T_J ≤ T_{HIGH}		-	2.3	3	°C/W

3. Assembled in TO-3 package using eutectic die attach. Die form performance is dependent on die attach, substrate choice & assembly method.

Typical Electrical Characteristics, T_J = 25°C (unless noted otherwise)

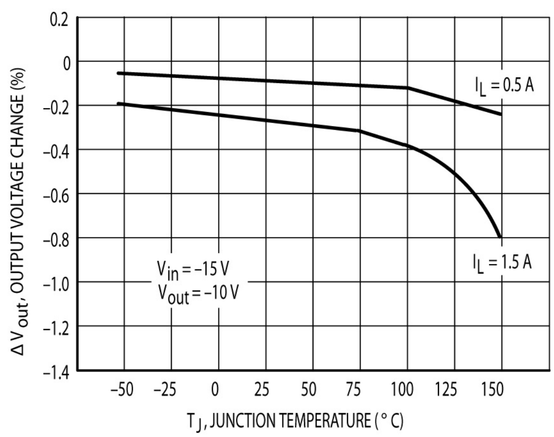


Figure 1 – Load Regulation

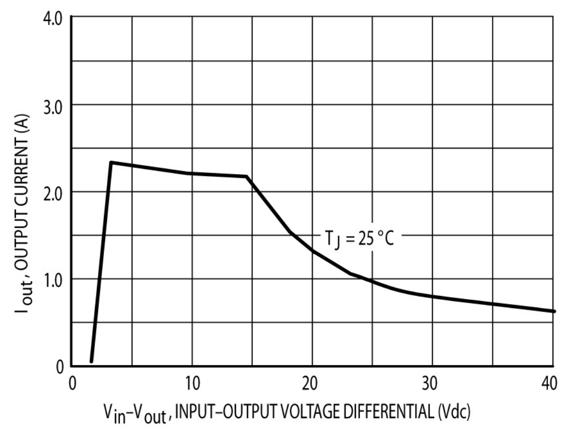


Figure 2 – Current Limit

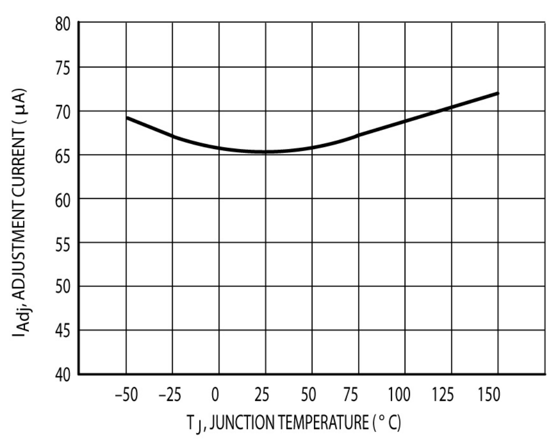


Figure 3 – Adjustment Pin Current

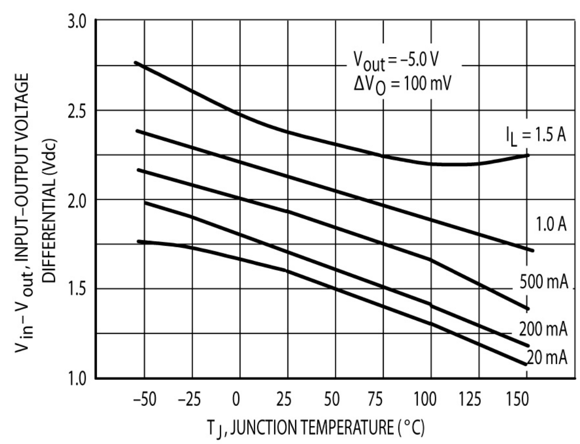


Figure 4 – Dropout Voltage

Typical Electrical Characteristics, T_J = 25°C (unless noted otherwise)

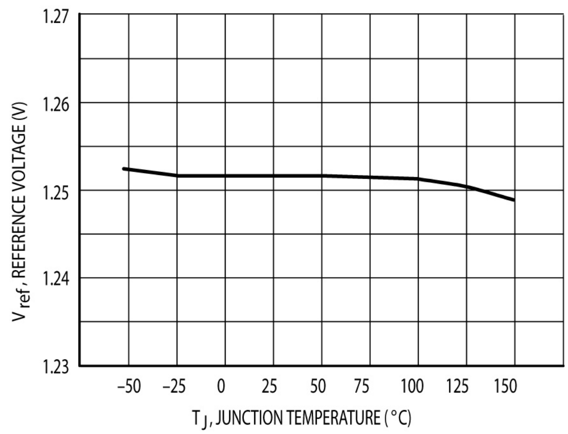


Figure 5 – Temperature Stability

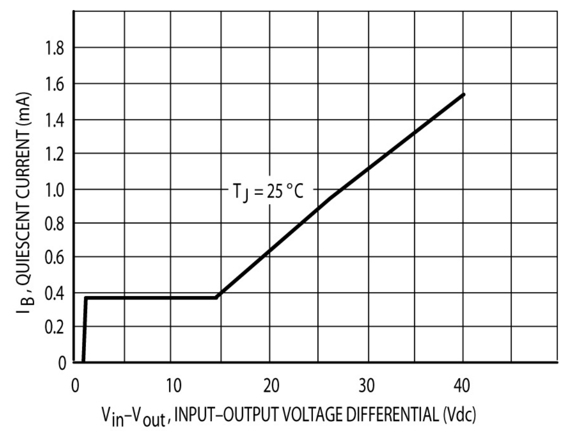


Figure 6 – Minimum Operating Current

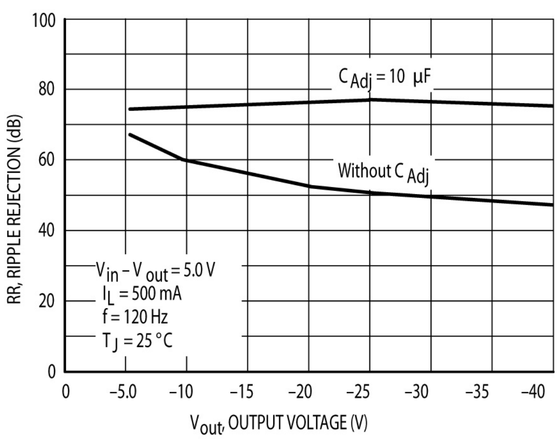


Figure 7 – Ripple Rejection versus Output Voltage

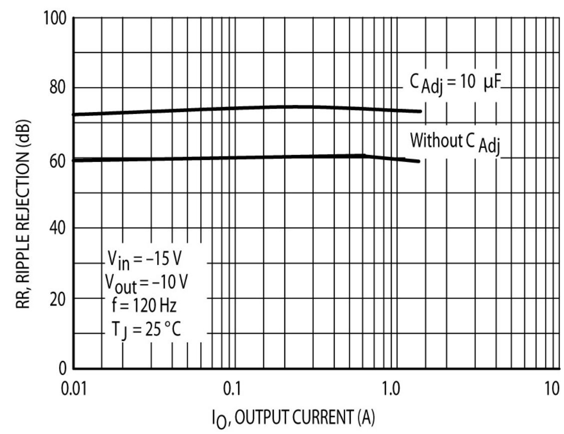


Figure 8 – Ripple Rejection versus Output Current

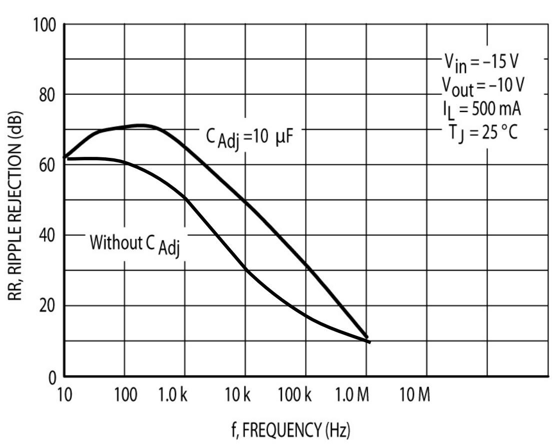


Figure 9 – Ripple Rejection versus Frequency

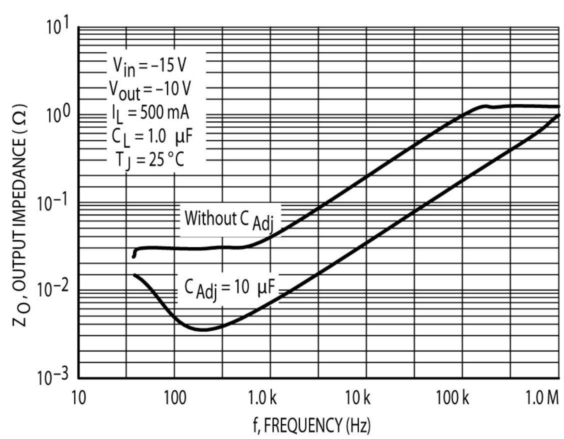


Figure 10 – Output Impedance

Typical Electrical Characteristics, T_J = 25°C (unless noted otherwise)

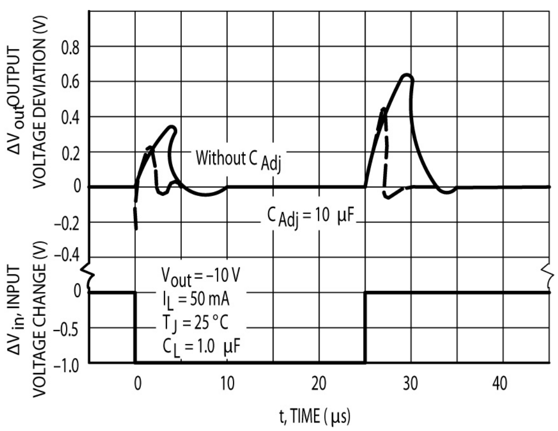


Figure 11– Line Transient Response

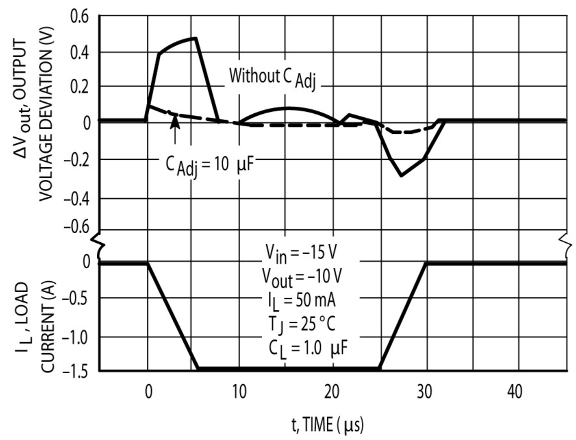


Figure 12– Load Transient Response