CMOS High Voltage Logic – CD4541B

Programmable Timer in bare die form

Rev 1.0
11/06/20

Description

The CD4541B programmable timer consists of a 16-stage binary counter, integrated oscillator for use with an external capacitor and x2 resistors, an automatic power-on reset circuit and output control logic. Power-on triggers automatic reset circuitry to initialize all counters. With power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16−stage counter divides the oscillator frequency (f_{osc}) with the nth stage frequency being $f_{osc}/2^n$. Counter increments on positive clock edge.

Features:

- Available outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Built-in low-power RC oscillator ≈ DC to 100kHz
- External clock option (Pad 3) overrides oscillator
- Use as 2^n frequency divider or single transition timer
- $Q/\overline{Q}$ select provides output logic level flexibility
- Auto or master reset disables oscillator for lower P_D
- CD4K process benefits: Wide supply voltage range; Symmetrical outputs; Low I_Q; High noise immunity
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

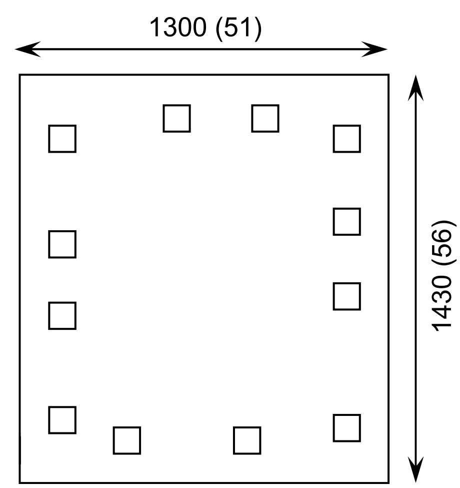
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



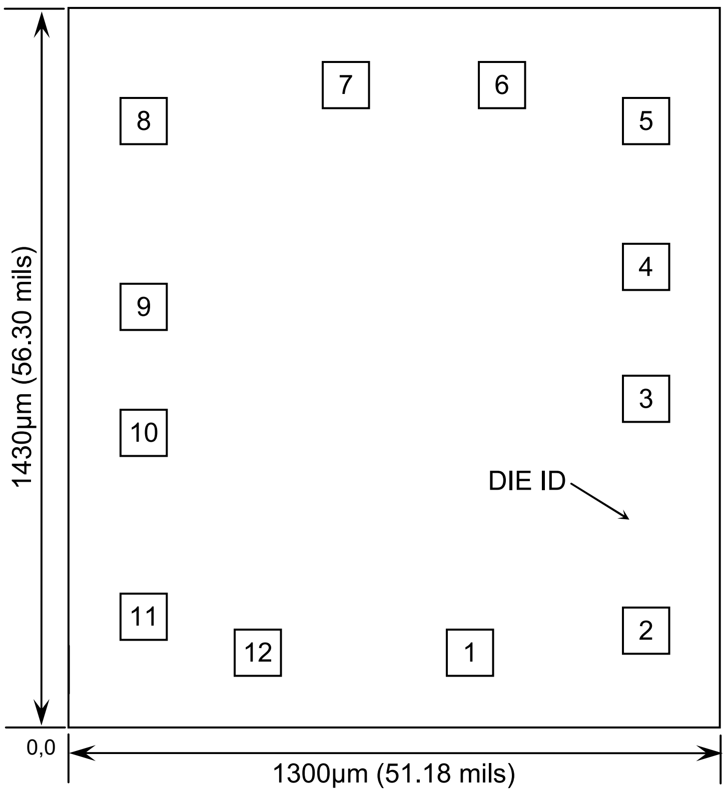
Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1300 x 1430 51 x 56	µm mils
Minimum Bond Pad Size	85 x 85 3.35 x 3.35	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	R_{tc}	0.7505	0.1080
2	C_{tc}	1.1070	0.1530
3	R_S	1.1070	0.6115
4	AR	1.1070	0.8745
5	MR	1.1070	1.1690
6	V_{SS}	0.8225	1.2370
7	Q	0.512	1.2370
8	Q / $\overline{Q}$ SELECT	0.1080	1.1635
9	MODE	0.1080	0.7955
10	A	0.1080	0.5495
11	B	0.1080	0.1815
12	V_{DD}	0.3345	0.1080
CONNECT CHIP BACK TO V_{DD} OR FLOAT			

Truth Table

PAD	STATE	
	0	1
4 AUTO RESET	AUTO RESET OPERATING	AUTO RESET DISABLED
5 MASTER RESET	TIMER OPERATIONAL	MASTER RESET ON
8 Q / Q	OUTPUT INITIALLY LOW AFTER RESET	OUTPUT INITIALLY HIGH AFTER RESET
9 MODE	SINGLE CYCLE MODE	RECYCLE MODE

Frequency Selection Table

A	B	Number of Counter stages "n"	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5 to +20	V
DC Input or Output Voltage (Referenced to V_{SS})	V_{IN}, V_{OUT}	-0.5 to V_{DD} +0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current or Output Current (per Pad)	I_{IN}, I_{OUT}	±10	mA
Power Dissipation in Still Air[2]	P_D	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3.0	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IN} = 0 or V_{DD}	4.95	4.95	4.95	V
		10V	V_{IN} = 0 or V_{DD}	9.95	9.95	9.95	
		15V	V_{IN} = 0 or V_{DD}	14.95	14.95	14.95	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IN} = V_{DD} or 0	0.05	0.05	0.05	V
		10V	V_{IN} = V_{DD} or 0	0.05	0.05	0.05	
		15V	V_{IN} = V_{DD} or 0	0.05	0.05	0.05	
Minimum High-Level Input Voltage	V_{IH}	5V	V_O = 0.5 or 4.5V	3.5	3.5	3.5	V
		10V	V_O = 1.0 or 9.0V	7.0	7.0	7.0	
		15V	V_O = 1.5 or 13.5V	11	11	11	
Maximum Low-Level Input Voltage	V_{IL}	5V	V_O = 4.5 or 0.5V	1.5	1.5	1.5	V
		10V	V_O = 9.0 or 1.0V	3.0	3.0	3.0	
		15V	V_O = 13.5 or 1.5V	4.0	4.0	4.0	
Minimum Output (Source) Current	I_{OH}	5V	V_{OH} = 2.5V	-6.2	-5	-3	mA
		5V	V_{OH} = 4.6V	-1.9	-1.55	-1.08	
		10V	V_{OH} = 9.5V	-5	-4	-2.8	
		15V	V_{OH} = 13.5V	-12.6	-10	-7.2	

4. -55°C ≤ T_J ≤ +125°C

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Output (Sink) Current	I_{OL}	5V	V_{OL} = 0.4V	1.9	1.55	1.08	mA
		10V	V_{OL} = 0.5V	5	4	2.8	
		15V	V_{OL} = 1.5V	12.6	10	7.2	
Maximum Input Leakage Current	I_{IN}	15V	V_{IN} = V_{DD} or V_{SS}	±0.1	±0.1	±1.0	μA
Maximum Quiescent Current[5]	I_{DD}	5V	V_{IN} = V_{DD} or V_{SS}	5	5	150	μA
		10V		10	10	300	
		15V		20	20	600	
		20V		100	100	3000	

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency (Figure 1)	f_{max}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	1.5	1.5	0.75	MHz
		10V		4	4	2	
		15V		6	6	3	
Maximum Propagation Delay, Clock to Q, $\overline{Q}$ (Figure 1)	2^8, t_{PLH}, t_{PHL}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	10.5	10.5	21	μs
		10V		3.8	3.8	7.6	
		15V		2.9	2.9	5.8	
	2^{16}, t_{PLH}, t_{PHL}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	18	18	36	μs
		10V		10	10	20	
		15V		7.5	7.5	15	
Maximum Output Transition Time, Any Output (Fig 1.)	t_{TLH}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	360	360	720	ns
		10V		180	180	360	
		15V		130	130	260	
Maximum Output Transition Time, Any Output (Fig. 1)	t_{THL}	5V	C_L = 50pF, R_L = 200kΩ t_r = t_f = 20ns	200	200	400	ns
		10V		100	100	200	
		15V		80	80	160	
Maximum Input Capacitance	C_{IN}	-	T_A = 25°C V_{IN} = 0V	7.5	7.5	7.5	pF

5. With AUTO RESET enable additional current drain at 25°C is:
200μA (Max) at 5V;
350μA (Max) at 10V;
500μA (Max) at 15V.

6. Not production tested in die form, characterized by chip design and tested in package.

Timing Requirements[6]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Pulse Width, Master Reset or Clock	t_w	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	900	1800	1800	ns
		10V		300	600	600	
		15V		225	450	450	
Maximum Rise and Fall Time, Clock (Figure 1)	t_r, t_f	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	Unlimited			μs
		10V					
		15V					

Operating Characteristics

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master-Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto-Reset pin when set to a "1" provides a low power operation. The RC oscillator will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3\, R_{tc} C_{tc}} \quad \text{if } (1\text{ kHz} \le f \le 100\text{ kHz})$$

and $R_S \approx 2\, R_{tc}$ where $R_S \ge 10$ kΩ

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13}, and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represent the Q output of the Nth stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip−flop (see Expanded Logic Diagram) resets, counting commences, and after 2^{n-1} counts the RS flip−flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

Switching Waveform

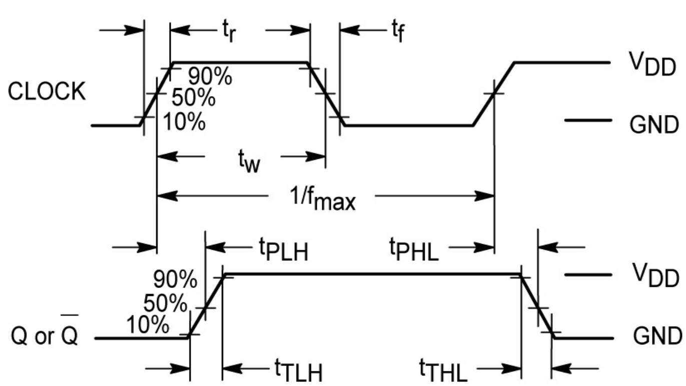
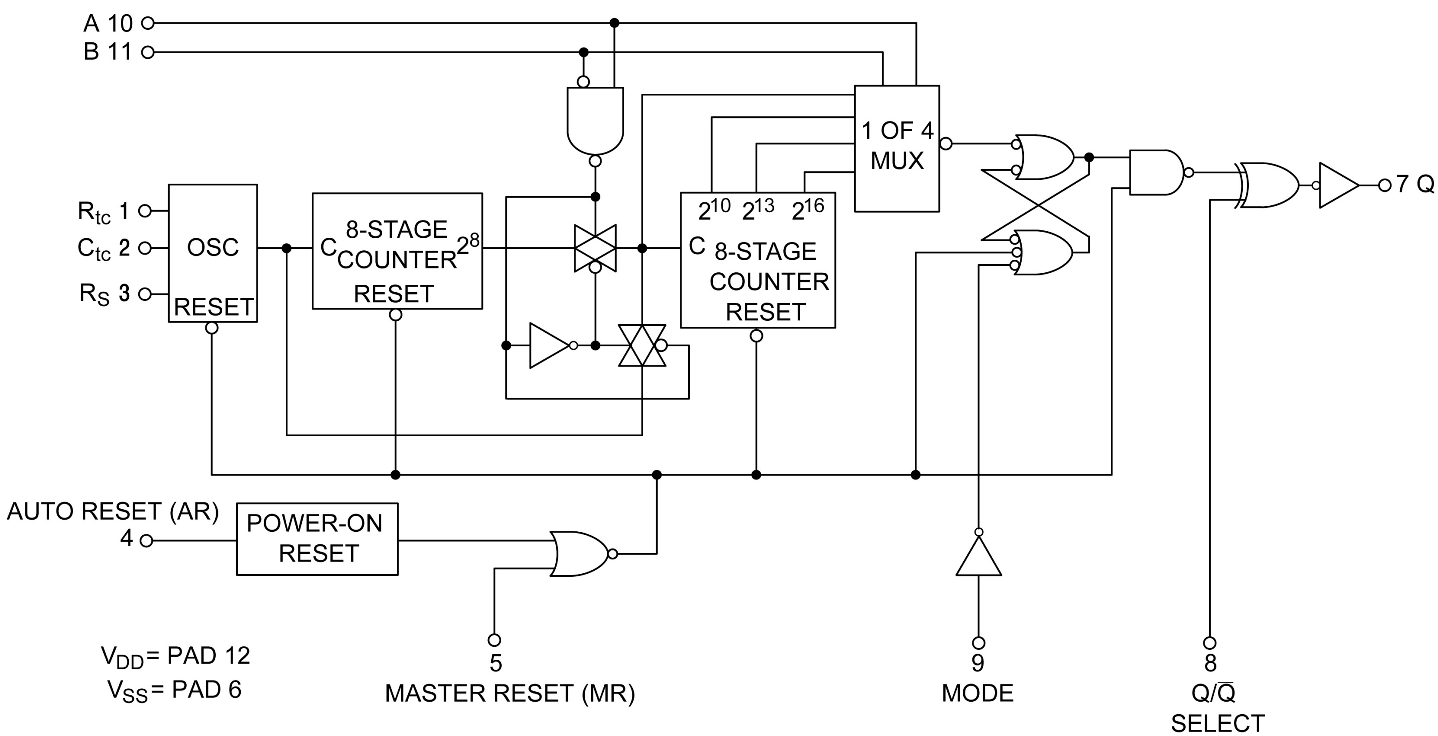


Figure 1 – Propagation Delay, Output Timing

Expanded Logic Diagram



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