



# CMOS High Voltage Logic – CD4073B

Triple 3-Input AND Gate Logic IC in bare die form

Rev 1.0  
15/03/18

## Description

The CD4073B Triple 3-Input AND Gate is fabricated using a 3µm 15CMOS process. This device consists of three independent circuits providing the system designer with direct implementation of the AND function. The device primarily finds use where high input voltage, low power dissipation and/or high noise immunity is desired. Inputs are protected against ESD and voltage transients by diode clamps to  $V_{DD}$  and  $V_{SS}$ .

## Features:

- High Input Voltage up to 20V
- Drives x2 Low-Power TTL loads or x1 LSTTL load
- Symmetrical Sink & Source Currents
- All outputs buffered
- Direct drop-in replacement for obsolete components in long term programs.

## Ordering Information

The following part suffixes apply:

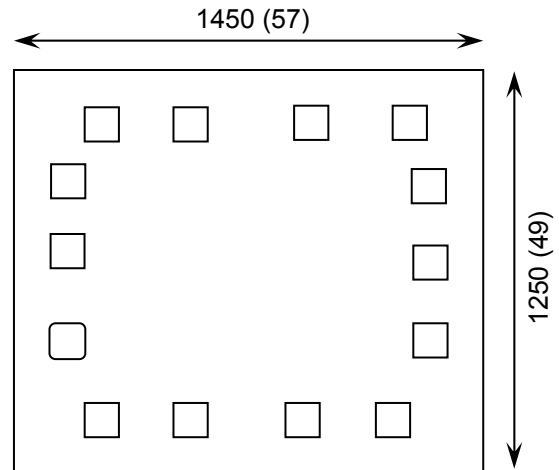
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

## Die Dimensions in µm (mils)



## Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1450 x 1250 57 x 49	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

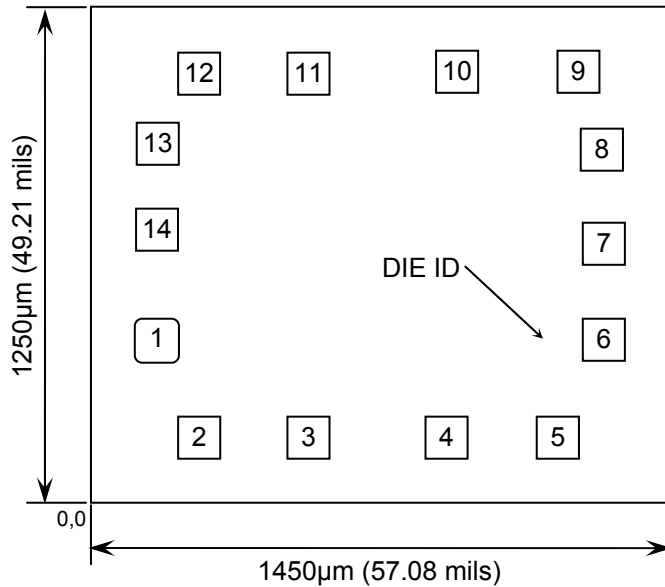




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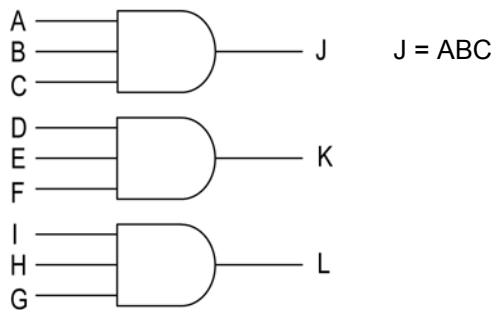
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A	0.1160	0.3630
2	B	0.2185	0.1160
3	D	0.4915	0.1160
4	E	0.8445	0.1160
5	F	1.1175	0.1160
6	K	1.2340	0.3630
7	V <sub>SS</sub>	1.2340	0.6065
8	C	1.2340	0.8405
9	J	1.1175	1.0340
10	L	0.8705	1.0340
11	I	0.4915	1.0340
12	H	0.2185	1.0340
13	G	0.1160	0.8515
14	V <sub>DD</sub>	0.1160	0.6410

CONNECT CHIP BACK TO V<sub>DD</sub> OR FLOAT

## Logic Diagram



## Truth Table

INPUTS			OUTPUT
A	B	C	J
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High level (steady state)  
L = Low level (steady state)  
X = Either Low or High level





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to $V_{SS}$ )	$V_{DD}$	-0.5 to +20	V
DC Input or Output Voltage (Referenced to $V_{SS}$ )	$V_{IN}, V_{OUT}$	-0.5 to $V_{DD}+0.5$	V
Storage Temperature Range	$T_{STG}$	-65 to 150	°C
Input Current or Output Current (per Pad)	$I_{IN}, I_{OUT}$	±10	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to $V_{SS}$ )

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{DD}$	3.0	18	V
DC Input Voltage, Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{DD}$	V
Operating Temperature Range	$T_J$	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $V_{SS} \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages referenced to $V_{SS}$ )

PARAMETER	SYMBOL	$V_{DD}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Output Voltage	$V_{OH}$	5V	$V_{IN} = 0 \text{ or } V_{DD}$	4.95	4.95	4.95	V
		10V	$V_{IN} = 0 \text{ or } V_{DD}$	9.95	9.95	9.95	
		15V	$V_{IN} = 0 \text{ or } V_{DD}$	14.95	14.95	14.95	
Maximum Low-Level Output Voltage	$V_{OL}$	5V	$V_{IN} = V_{DD} \text{ or } 0$	0.05	0.05	0.05	V
		10V	$V_{IN} = V_{DD} \text{ or } 0$	0.05	0.05	0.05	
		15V	$V_{IN} = V_{DD} \text{ or } 0$	0.05	0.05	0.05	
Minimum High-Level Input Voltage	$V_{IH}$	5V	$V_O = 0.5 \text{ or } 4.5V$	3.5	3.5	3.5	V
		10V	$V_O = 1.0 \text{ or } 9.0V$	7.0	7.0	7.0	
		15V	$V_O = 1.5 \text{ or } 13.5V$	11	11	11	
Maximum Low-Level Input Voltage	$V_{IL}$	5V	$V_O = 4.5 \text{ or } 0.5V$	1.5	1.5	1.5	V
		10V	$V_O = 9.0 \text{ or } 1.0V$	3.0	3.0	3.0	
		15V	$V_O = 13.5 \text{ or } 1.5V$	4.0	4.0	4.0	
Minimum Output (Source) Current	$I_{OH}$	5V	$V_{OH} = 2.5V$	-3.0	-2.4	-1.7	mA
		5V	$V_{OH} = 4.6V$	-0.64	-0.51	-0.36	
		10V	$V_{OH} = 9.5V$	-1.6	-1.3	-0.9	
		15V	$V_{OH} = 13.5V$	-4.2	-3.4	-2.4	

4.  $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$





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## DC Electrical Characteristics (Voltages referenced to $V_{SS}$ )

PARAMETER	SYMBOL	$V_{DD}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum Output (Sink) Current	$I_{OL}$	5V	$V_{OL} = 0.4V$	0.64	0.51	0.36	mA
		10V	$V_{OL} = 0.5V$	1.6	1.3	0.9	
		15V	$V_{OL} = 1.5V$	4.2	3.4	2.4	
Maximum Input Leakage Current	$I_{IN}$	15V	$V_{IN} = V_{DD}$ or $V_{SS}$	$\pm 0.1$	$\pm 0.1$	$\pm 1.0$	$\mu A$
Maximum Quiescent Current	$I_{DD}$	5V	$V_{IN} = V_{DD}$ or $V_{SS}$	0.25	0.25	7.5	$\mu A$
		10V		0.5	0.5	15	
		15V		1.0	1.0	30	

## AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	$V_{DD}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Input to Output (Figure 1)	$t_{PLH}, t_{PHL}$	5V	$C_L = 50pF,$ $R_L = 200k\Omega$ $t_r = t_f = 20ns$	250	250	500	ns
		10V		120	120	240	
		15V		90	90	180	
Maximum Output Transition Time, Any Output (Figure 1)	$t_{TLH}, t_{THL}$	5V	$C_L = 50pF,$ $R_L = 200k\Omega$ $t_r = t_f = 20ns$	200	200	400	ns
		10V		100	100	200	
		15V		80	80	160	
Maximum Input Capacitance	$C_{IN}$	-	$T_A = 25^\circ C$ $V_{IN} = 0V$	TYPICAL			pF
				-	5	-	

5. Not production tested in die form, characterized by chip design and tested in package.

## Switching Waveform

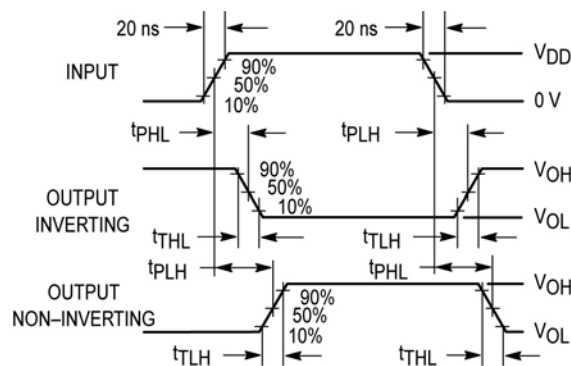


Figure 1 – Propagation Delay, Output Timing





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