CMOS High Voltage Logic – CD4053B

Triple 2-Channel Analog Multiplexer/Demultiplexer in bare die form

Rev 1.0
08/09/18

Description

The CD4053B is a digitally controlled Analog Switch consisting of x3 separate digital control inputs, A, B, & C plus inhibit input. Each control input selects one of a pair of channels in SPDT configuration. Logic "1" at the inhibit input switches all channels off. Logic-level conversion of analog signals up to $18V_{P-P}$ is achieved via digital signal amplitudes of 4.5V to 18V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} up to 13V can be controlled; for V_{DD}-V_{EE} level differences >13V, V_{DD}-V_{SS} ≥ 4.5V is required). Featuring low ON impedance & very low OFF leakage current, quiescent power consumption is extremely low across the full V_{DD}-V_{SS} & V_{DD}-V_{EE} range and independent of control logic state.

Features:

- Break-before-make switch function eliminates channel overlap
- Supply voltage range: 3V to 18V
- Analog voltage range (V_{DD} - V_{EE}) : 3V to 18V
- ON resistance: 125Ω (typ) over $15V_{P-P}$ signal
- Channel leakage current: 100 nA ,V_{DD} = 18V
- Matched Switch Characteristics: R_{ON} = 10Ω (max), V_{DD} - V_{EE} = 15V
- Quiescent current : 0.2 µA, V_{DD} = 15V
- Binary address decoding on-chip

Ordering Information

The following part suffixes apply:

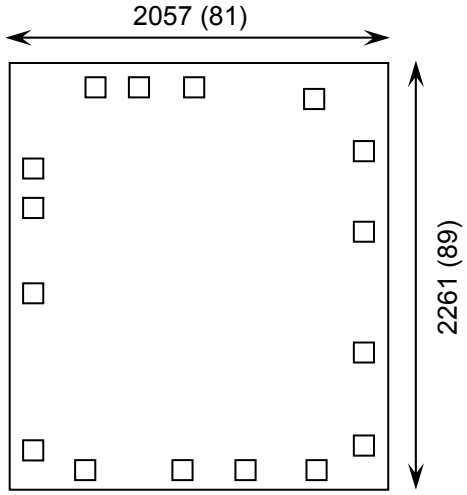
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 635µm(25 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	2057 x 1850 81 x 89	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	635 (±20) 25 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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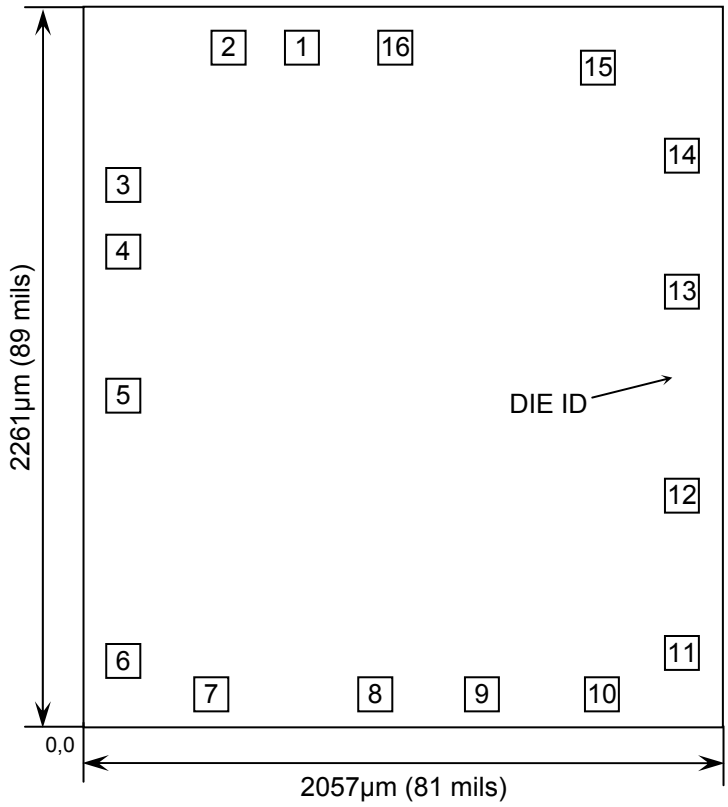
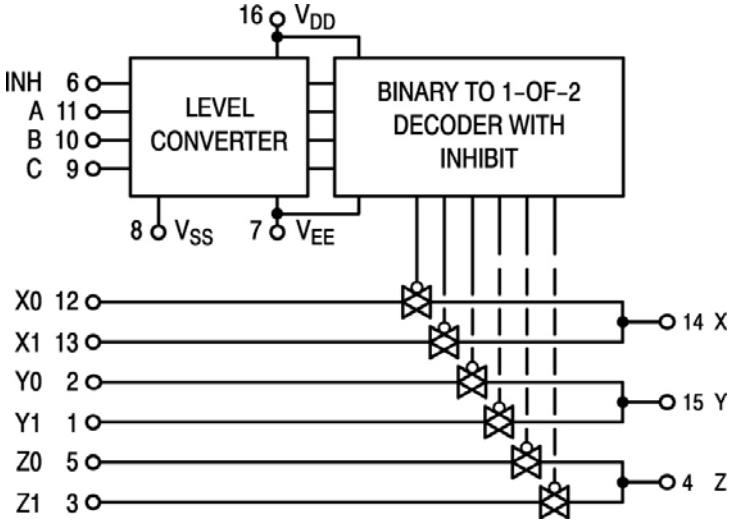
Pad Layout and Functions



PAD	FUNCTION
1	Y1 IN / OUT
2	Y0 IN / OUT
3	Z1 IN / OUT
4	Z OUT / IN
5	Z0 IN / OUT
6	INH
7	V_{EE}
8	V_{SS}
9	C SELECT
10	B SELECT
11	A SELECT
12	X0 IN / OUT
13	X1 IN / OUT
14	X OUT / IN
15	Y OUT / IN
16	V_{DD}
CONNECT CHIP BACK TO V_{DD} OR FLOAT	

Logic Diagram



Truth Table

CONTROL INPUTS						
INHIBIT	SELECT			ON SWITCHES		
	C	B	A			
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	NONE		

x = DON'T CARE

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	V_{DD}	-0.5 to +20	V
DC Input or Output Voltage (Referenced to V_{SS} for control inputs and V_{EE} for switch I/O)	V_{IN}, V_{OUT}	-0.5 to V_{DD} +0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current or Output Current (per Pad)	I_{IN}, I_{OUT}	±10	mA
Power Dissipation in Still Air	P_D	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics Control Inputs Inhibit, A, B, C (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	5V	V_{IS} = V_{DD} thru 1kΩ, V_{EE} = GND =0, I_{IS} <2μA on all off channels, R_L =1kΩ to GND	3.5	3.5	3.5	V
		10V		7	7	7	
		15V		11	11	11	
Maximum Low-Level Input Voltage	V_{IL}	5V		1.5	1.5	1.5	V
		10V		3	3	3	
		15V		4	4	4	
Maximum Input Leakage Current	I_{IN}	18V	V_{IN} = V_{DD} or GND, V_{EE} = GND = 0	±0.1	±0.1	±1.0	μA

4. $-55^{\circ}C \leq T_J \leq +125^{\circ}C$.

DC Electrical Characteristics Switches in/out & common out/in X,Y,Z (Voltages referenced to V_{EE})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum "ON" Resistance	R_{ON}	5V	V_{EE} = V_{DD} or GND, V_{IS} = GND to V_{DD}	800	1050	1150	Ω
		10V		310	400	550	
		15V		200	240	320	

DC Electrical Characteristics Switches in/out, Common out/in X,Y,Z (Voltages referenced to V_{EE})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum difference in "ON" resistance between any two channels	ΔR_{ON}	5V	V_{EE} = GND = 0	25	70	135	Ω
		10V		25	50	95	
		15V		10	45	65	
Maximum off-channel leakage current, any one channel or common channel	I_{OFF}	18V	V_{EE} = GND = 0	±100	±100	±1000	nA

DC Electrical Characteristics Supply Characteristics (Voltages referenced to V_{EE})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum quiescent supply current	I_{DD}	5V	Channel Select = V_{DD} or GND, V_{EE} = GND = 0	5	5	150	nA
		10V		10	10	300	
		15V		15	20	600	
		20V		100	100	3000	

AC Electrical Characteristics[5] (C_L = 50pF, Input $t_r = t_f$ = 20ns)

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Max. propagation delay, Analog Input to Analog Output	t_{PHL}, t_{PLH}	5V	R_L =200kΩ, V_{EE} = GND = 0	60	60	70	ns
		10V		30	30	40	
		15V		20	20	30	
Max. propagation delay, Channel-Select Input to Analog Output (Figure 2)	t_{PHL1}, t_{PLH1}	5V	R_L =200kΩ, V_{EE} = GND = 0	350	350	400	ns
		10V		200	200	250	
		15V		160	160	200	
	t_{PZL1}, t_{PZH1} t_{PLZ1}, t_{PHZ1}	5V	R_L =10kΩ, V_{EE} = GND = 0	720	720	720	ns
		10V		320	320	320	
		15V		240	240	240	
		5V	V_{EE} = -5V, GND =0	450	450	450	
Max. Propagation Delay, Inhibit to Analog Output (Figure 2)	t_{PZL2}, t_{PZH2}	5V	R_L =10kΩ, V_{EE} = GND = 0	720	720	720	ns
		10V		320	320	320	
		15V		240	240	240	
	t_{PLZ2}, t_{PHZ2}	5V	R_L =1kΩ, V_{EE} = GND = 0	450	450	450	ns
		10V		210	210	210	
		15V		160	160	160	
		5V	V_{EE} = -10V,GND =0	300	300	600	

AC Electrical Characteristics[5] (C_L = 50pF, Input t_r = t_f = 20ns, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Max. Input Capacitance, Select / Inhibit	C_{IN}	-	-	-	7.5	-	pF
Input / Output Capacitance				TYPICAL			pF
	C_{IS}	5V	V_{EE} = GND = -5V	-	5	-	
	C_{OS}	5V		-	9	-	
	C_{IOS}	5V		-	0.2	-	

5. Not production tested in die form, characterized by chip design and tested in package.

Signal Characteristics[5] (C_L = 50pF, Input t_r = t_f = 20ns, T_J = 25°C unless otherwise specified)

PARAMETER	SYMBOL	V_{DD}	V_{IS}[6]	CONDITIONS		TYPICAL	UNITS
-3dB Maximum input On-channel bandwidth or minimum frequency response	B_W	10V	2.5V	V_{EE} = GND =0, R_L=1kΩ, 20 log(V_{OS}/V_{IS}) = -3dB	V_{OS} at Common OUT/IN	30	MHz
					V_{OS} at any channel	60	
-40dB Feed-through frequency (All channels off)	f_1	10V	2.5V	V_{EE} = GND =0, R_L=1kΩ, 20 log(V_{OS}/V_{IS})= -40dB	V_{OS} at Common OUT/IN	8	MHz
					V_{OS} at any channel	8	
-40dB Signal crosstalk frequency between sections	f_2	10V	2.5V	V_{EE} = GND =0, R_L=1kΩ, 20 log(V_{OS}/V_{IS})= -40dB	In pad 2, out pad 14	2.5	MHz
					In pad 15, out pad 14	6	
Total harmonic distortion	THD	5	1	V_{EE} = GND =0, f_{is} = 1kHZ sine wave		0.3	%
		10	1.5			0.2	
		15	2.5			0.12	
Address-or-enable to signal crosstalk	$V_{AO/I}$	10	-	V_{EE} = GND =0, R_L=10kΩ[7], Square wave		65	mV Peak

6. Peak-to peak voltage symmetrical as (V_{DD}-V_{EE})/2
7. Both ends of channel

Switching Waveforms

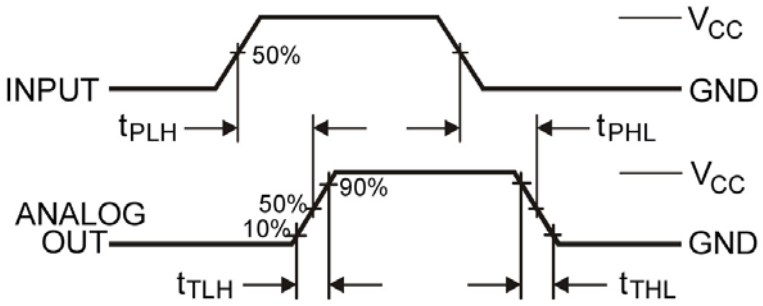

Figure 1 – Propagation Delay, Input to Analog Output

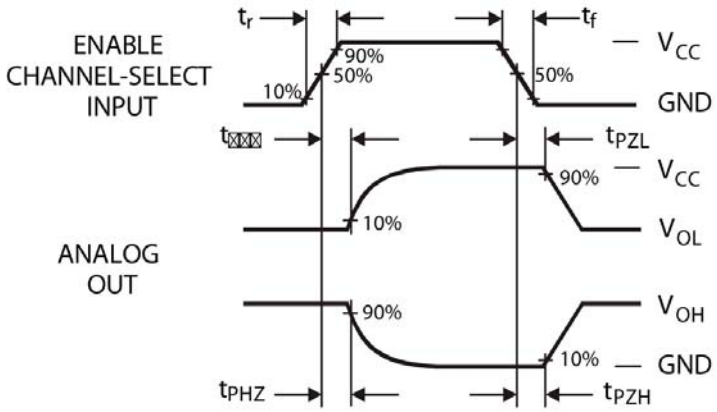

Figure 2 – Propagation Delay, Channel-Select Input to Analog Output