CMOS High Voltage Logic – CD4049UB

CMOS Hex Inverting Buffer / Converter in bare die form

Rev 1.0
18/09/18

Description

The CD4049UB features logic level conversion using only one supply voltage, V_{DD}. The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when this device is used for logic level conversion. This device is intended for use as a CMOS to DTL/TTL converter and can drive directly two DTL / TTL loads (V_{DD} =5V, $V_{OL} \leq 0.4V$, and $I_{OL} \geq 3.3mA$). The device finds primary use where low power dissipation and/or high noise immunity is desired. This part should be considered a preferable replacement for CD4009UB or CD4010B in any inverter, current driver, or logic level conversion application due to its single power supply capability.

Features:

- Supply voltage range: 3V to 18V
- High Source and Sink Currents
- V_{IN} can exceed V_{DD}
- High-to-Low Level Logic Conversion
- High Sink Current for Driving x2 TTL Loads
- Maximum Input Current: 1 µA at 18 V over full temperature range
- ESD protection diodes on all inputs

Ordering Information

The following part suffixes apply:

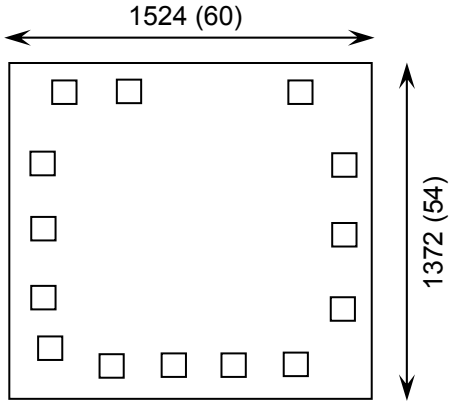
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 635µm(25 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1524 x 1372 60 x 54	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	635 (±20) 25 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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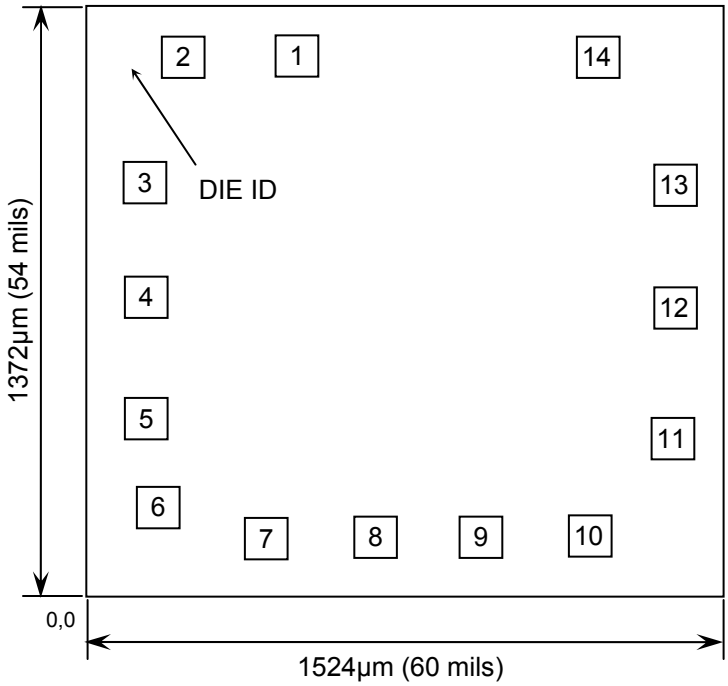
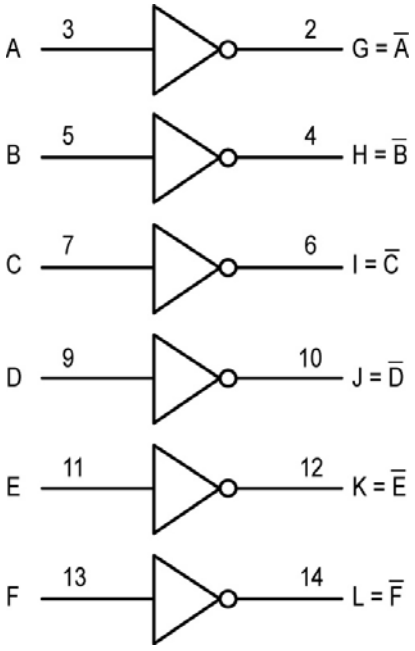
Pad Layout and Functions



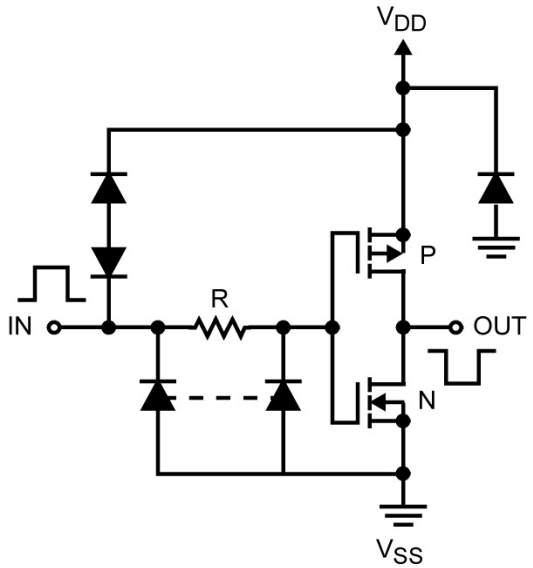
PAD	FUNCTION
1	V_{DD}
2	G = $\overline{A}$
3	A
4	H = $\overline{B}$
5	B
6	I = $\overline{C}$
7	C
8	V_{SS}
9	D
10	J = $\overline{D}$
11	E
12	K = $\overline{E}$
13	F
14	L = $\overline{F}$
CONNECT CHIP BACK TO V_{DD} OR FLOAT	

Logic Diagram



Pad 1 = V_{DD}
Pad 8 = V_{SS}

Schematic (1/6 of circuit)



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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5 to +20	V
DC Input Voltage (Referenced to V_{SS})	V_{IN}	-0.5 to +20	V
DC Output Voltage (Referenced to V_{SS})	V_{OUT}	-0.5 to V_{DD} +0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±10	mA
Output Current (per Pad)	I_{OUT}	±45	mA
Power Dissipation in Still Air	P_D	825	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	5V	V_{OUT} = 0.5V	4	4	4	V
		10V	V_{OUT} = 1V	8	8	8	
		15V	V_{OUT} = 1.5V	12.5	12.5	12.5	
Maximum Low-Level Input Voltage	V_{IL}	5V	V_{OUT} = 4.5V	1	1	1	V
		10V	V_{OUT} = 9V	2	2	2	
		15V	V_{OUT} = 13.5V	2.5	2.5	2.5	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IN} = V_{SS} or V_{DD}	4.95	4.95	4.95	V
		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IN} = V_{DD} or V_{SS}	0.05	0.05	0.05	V
		10V		0.05	0.05	0.05	
		15V		0.05	0.05	0.05	
Maximum Input Leakage Current	I_{IN}	15V	V_{IN} = V_{DD} or V_{SS}	±0.1	±.0.1	±1.0	µA

4. $-55^{\circ}C \le T_J \le +125^{\circ}C$

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DC Electrical Characteristics (Voltages referenced to V_{SS})

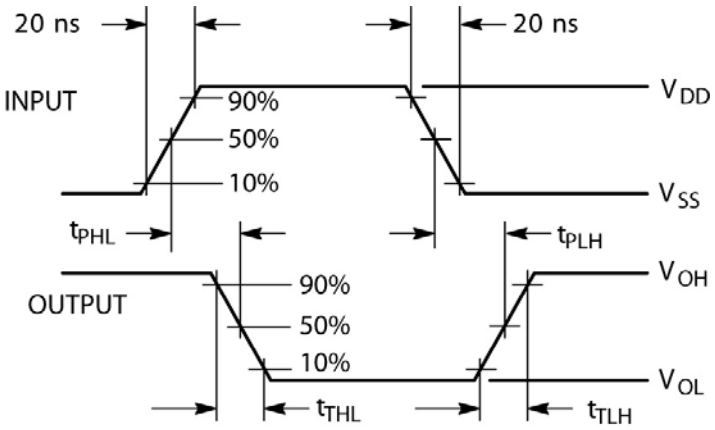
PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Quiescent Supply Current	I_{DD}	5V	$V_{IN} = V_{DD}$ or V_{SS} $I_{OUT} = 0\mu A$	1	1	30	µA
		10V		2	2	60	
		15V		4	4	120	

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{DD}	V_{IN}	CONDITIONS	TYPICAL	LIMITS	UNITS
Propagation Delay, Low to High	$t_{PLH,}$	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	60	120	ns
		10V	10V		32	65	
		15V	15V		25	50	
Output Propagation Delay, High to Low	t_{PHL}	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	32	65	ns
		10V	10V		20	40	
		15V	15V		15	30	
Transition Time, Low to High	$t_{TLH,}$	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	80	160	ns
		10V	10V		40	80	
		15V	15V		30	60	
Transition Time, High to Low	$t_{THL,}$	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	30	60	ns
		10V	10V		20	40	
		15V	15V		15	30	
Input Capacitance	C_{IN}	-		$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	15	22.5	pF

5. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform



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