CMOS High Voltage Logic – CD4046B

CMOS Micropower Phase Locked Loop (PLL) in bare die form

Rev 1.0
21/09/18

Description

The CD4046B phase locked loop consists of two phase comparators, a voltage-controlled oscillator (VCO), source follower and zener diode. The comparators have a common signal input amplifier and common comparator input. The zener diode is used for power supply regulation if required. Applications include FM and FSK modulation / demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

Features:

- Choice of two Phase Comparators:
  - Exclusive Or Gate, duty cycle limited
  - Rising edge switching, duty cycle unlimited
- Buffered outputs compatible with MHTL and Low power TTL
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Source-follower output of VCO control input
- Integrated zener diode to assist supply regulation
- Supply voltage range: 3V to 18V
- Symmetrical output characteristics

Ordering Information

The following part suffixes apply:

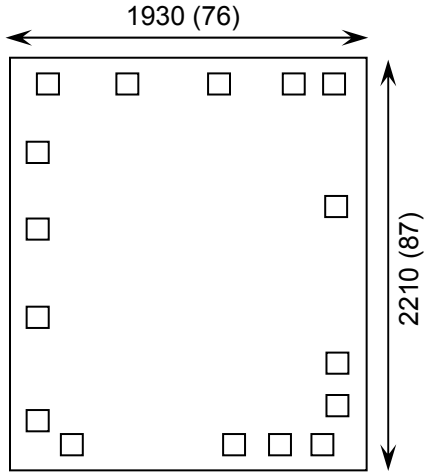
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 635µm(25 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1930 x 2210 76 x 87	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	635 (±20) 25 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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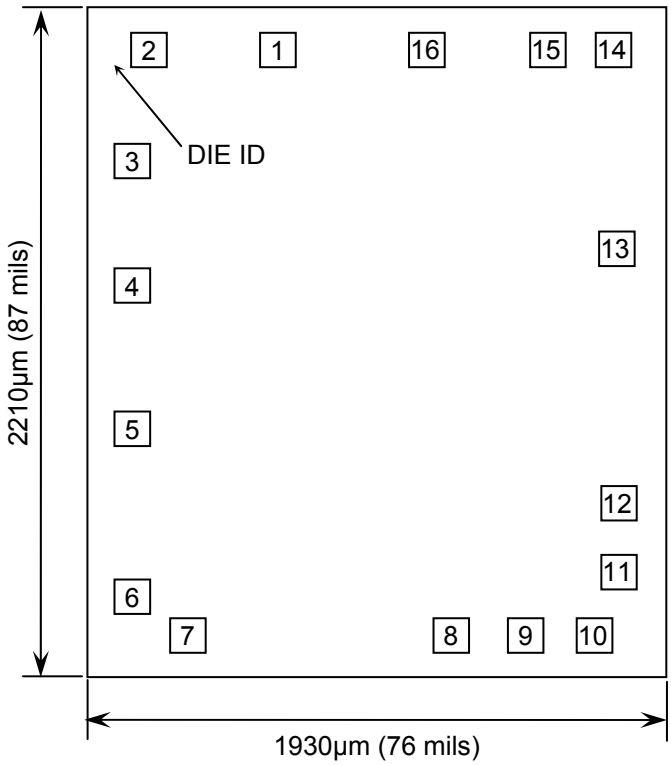
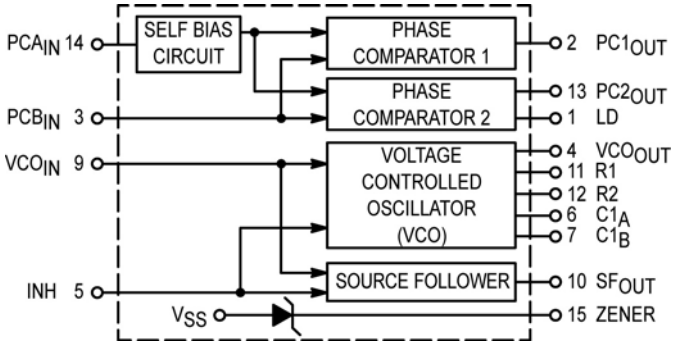
Pad Layout and Functions



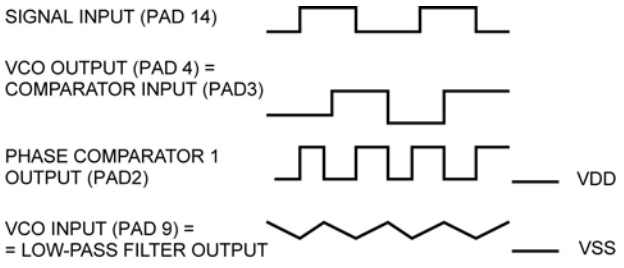
PAD	FUNCTION
1	LD
2	$PC1_{OUT}$
3	PCB_{IN}
4	VCO_{OUT}
5	INH
6	$C1_A$
7	$C1_B$
8	V_{SS}
9	VCO_{IN}
10	SF_{OUT}
11	R1
12	R2
13	$PC2_{OUT}$
14	PCA_{IN}
15	ZENER
16	V_{DD}
CONNECT CHIP BACK TO V_{DD} OR FLOAT	

Block Diagram



Pad 1 = V_{DD}
Pad 8 = V_{SS}

PLL Waveforms



Typical waveforms for CMOS PLL with phase comparator in locked condition of f_{osc}

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5 to +20	V
DC Input Voltage (Referenced to V_{SS})	V_{IN}	-0.5 to V_{DD} +0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±10	mA
Power Dissipation in Still Air	P_D	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_A	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	5V	V_{OUT} = 0.5V or 4.5V	3.5	3.5	3.5	V
		10V	V_{OUT} = 1V or 9V	7	7	7	
		15V	V_{OUT} = 1.5V or 13.5V	11	11	11	
Maximum Low-Level Input Voltage	V_{IL}	5V	V_{OUT} = 4.5V or 0.5V	1.5	1.5	1.5	V
		10V	V_{OUT} = 9V or 1V	3	3	3	
		15V	V_{OUT} = 13.5V or 1.5V	4.0	4.0	4.0	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IN} = 0 or V_{DD}	4.95	4.95	4.95	V
		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IN} = V_{DD} or 0	0.05	0.05	0.05	V
		10V		0.05	0.05	0.05	
		15V		0.05	0.05	0.05	
Maximum Input Leakage Current	I_{IN}	15V	V_{IN} = V_{DD} or V_{SS}	±0.1	±.0.1	±1.0	µA

4. $-55^{\circ}C \le T_J \le +125^{\circ}C$

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DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Output Drive (Source)	I_{OH}	5	V_{OH} = 2.5V	-1.2	-1.0	-0.7	mA
		5	V_{OH} = 4.6V	-0.25	-0.2	-0.14	
		10	V_{OH} = 9.5V	-0.65	-0.5	-0.35	
		15	V_{OH} = 13.5V	-1.8	-1.5	-1.1	
Minimum Output Drive (Sink)	I_{OL}	5	V_{OL} = 0.4V	0.64	0.51	0.36	mA
		10	V_{OL} = 0.5V	1.6	1.3	0.9	
		15	V_{OL} = 1.5V	4.2	3.4	2.4	
Maximum Quiescent Supply Current	I_{DD}	5V	INH = PCA_{IN} = V_{DD}, Zener = VCO_{IN} = 0V, PCB_{IN} = V_{DD} or 0V, I_{OUT} = 0µA	5	5	150	µA
		10V		10	10	300	
		15V		20	20	600	
Noise Immunity Margin	-	5V	"1" & "0" level	1	-	-	V
		10V		1	-	-	
		15V		1	-	-	

AC Electrical Characteristics[5] T_J = 25°C unless otherwise specified

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	MIN	TYPICAL	MAX	UNITS
Transition Time, Low to High	t_{TLH}	5V	C_L = 50pF	-	180	350	ns
		10V		-	90	150	
		15V		-	65	110	
Transition Time, High to Low	t_{THL}	5V	C_L = 50pF	-	100	175	ns
		10V		-	50	75	
		15V		-	37	55	
PHASE COMPARATORS 1 AND 2							
PARAMETER	**SYMBOL**	**V_{DD}**	**CONDITIONS**	**MIN**	**TYPICAL**	**MAX**	**UNITS**
Input Resistance	R_{IN}	5V	PCA_{IN}	1.0	2.0	-	MΩ
		10V		0.2	0.4	-	
		15V		0.1	0.2	-	
		15V	PCB_{IN}	150	1500	-	
Minimum Input Sensitivity	V_{IN}	5V	AC coupled - PCA_{IN}, C Series = 1000pF, f = 50kHz	-	200	300	mV p-p
		10V		-	400	600	
		15V		-	700	1050	
		5 -15V	DC coupled,PCA_{IN},PCB_{IN}	See noise immunity			
VOLTAGE CONTROLLED OSCILLATOR (VCO)							
Maximum Frequency	f_{MAX}	5V	VCO_{IN} = V_{DD}, C1 = 50pF, R1 = 5kΩ, R2 = ∞	0.5	0.7	-	MHz
		10V		1.0	1.4	-	
		15V		1.4	1.9	-	

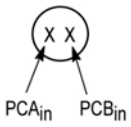
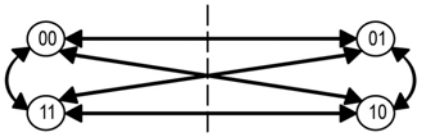
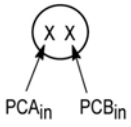
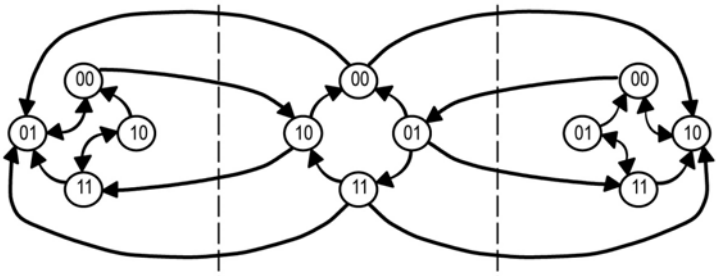
5. Not production tested in die form, characterized by chip design and tested in package.

AC Electrical Characteristics[5] T_J = 25°C unless otherwise specified

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	MIN	TYPICAL	MAX	UNITS
Temperature - Frequency stability	-	5V	R2 = ∞,	-	0.12	-	%/°C
		10V		-	0.04	-	
		15V		-	0.015	-	
Linearity	-	5V	R2 = ∞, VCO_{IN} = 2.5V ± 0.3V, R1 > 10kΩ	-	1	-	%
		10V	R2 = ∞, VCO_{IN} = 5V ± 2.5V, R1 > 400kΩ	-	1	-	
		15V	R2 = ∞, VCO_{IN} = 7.5V ± 5V, R1 ≥ 1000kΩ	-	1	-	
Output Duty Cycle	-	5 -15V	-	-	50	-	%
Input Resistance	R_{IN}	15	VCO_{IN}	150	1500	-	MΩ
SOURCE FOLLOWER							
PARAMETER	**SYMBOL**	**V_{DD}**	**CONDITIONS**	**MIN**	**TYPICAL**	**MAX**	**UNITS**
Offset Voltage	V_{OS}	5V	VCO_{IN} – SF_{OUT}, RSF > 500kΩ	-	1.65	2.2	V
		10V		-	1.65	2.2	
		15V		-	1.65	2.2	
Linearity	-	5V	VCO_{IN} = 2.5V ± 0.3V, RSF > 50kΩ	-	0.1	300	%
		10V	VCO_{IN} = 5V ± 2.5V, RSF > 50kΩ	-	0.6	600	
		15V	VCO_{IN} = 7.5V ± 5V, RSF > 50kΩ	-	0.8	1050	
ZENER DIODE							
Zener Voltage	V_Z	-	I_Z = 50µA	6.7	7	7.3	V
Dynamic Resistance	R_Z	-	I_Z = 1mA	-	100	-	Ω

5. Not production tested in die form, characterized by chip design and tested in package.

Phase Comparator State Diagram & Design Info

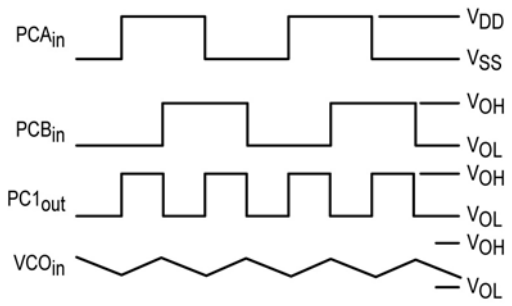
PHASE COMPARATOR 1			
Input Stage 			
PC1$_{out}$	0		1
PHASE COMPARATOR 2			
Input Stage 			
PC2$_{out}$	0	3–State Output Disconnected	1
LD (Lock Detect)	0	1	0

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$)	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low–pass filter characteristics (see low pass example). $f_C \leq f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.	$f_{min} = \frac{1}{R_2(C_1 + 32\ pF)}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32\ pF)} + f_{min}$ (V_{CO} input = V_{DD}) Where: $10K \leq R_1 \leq 1\ M$ $10K \leq R_2 \leq 1\ M$ $100pF \leq C_1 \leq .01\ \mu F$	

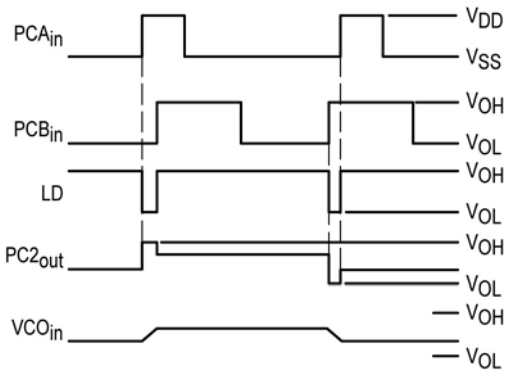
Refer to General Phase–Locked Loop Connections and Waveforms

General Phase–Locked Loop Connections and Waveforms

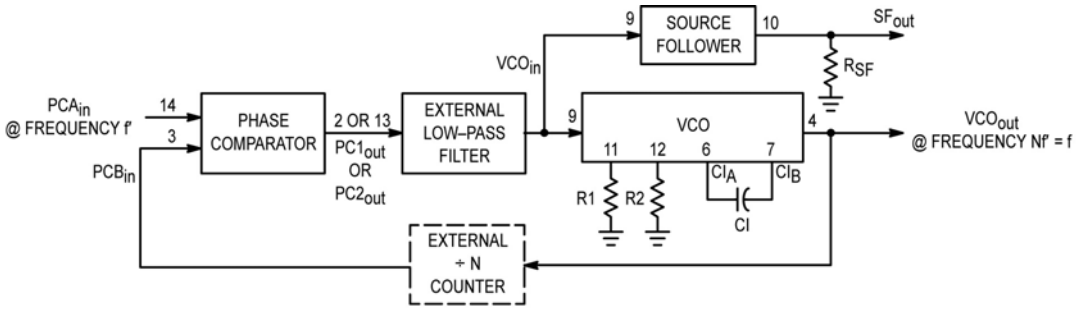
PHASE COMPARATOR 1



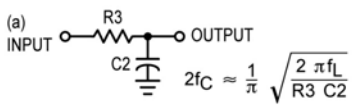
PHASE COMPARATOR 2

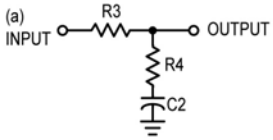


Low Pass Filter Example



Typical Low–Pass Filters





Typically:

$$R_4\ C_2 = \frac{6N}{f_{max}} - \frac{N}{2\ \pi\ \Delta\ f}$$

$$(R_3 + 3{,}000\Omega)\ C_2 = \frac{100N\Delta f}{f_{max}^2} - R_4\ C_2$$

$$\Delta f = f_{max} - f_{min}$$

NOTE: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor C_C is then placed from the midpoint to ground. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_n. In Figure B, the ratio of R3 to R4 sets the damping, R4 ≅ (0.1)(R3) for optimum results.

Definitions: N = Total division ratio in feedback loop
$K\varphi = V_{DD}/\pi$ for Phase Comparator 1
$K\varphi = V_{DD}/4\ \pi$ for Phase Comparator 2

$$K_{VCO} = \frac{2\ \pi\ \Delta\ f_{VCO}}{V_{DD} - 2\ V}$$

for a typical design $\omega_n \cong \frac{2\ \pi\ f_r}{10}$ (at phase detector input)

$\zeta \cong 0.707$

LOW–PASS FILTER

Filter A	Filter B
$\omega_n = \sqrt{\frac{K\varphi K_{VCO}}{NR_3C_2}}$	$\omega_n = \sqrt{\frac{K\varphi K_{VCO}}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\varphi K_{VCO}}$	$\zeta = 0.5\ \omega_n\ (R_3C_2 + \frac{N}{K\varphi K_{VCO}})$
$F(s) = \frac{1}{R_3C_2S + 1}$	$F(s) = \frac{R_3C_2S + 1}{S(R_3C_2 + R_4C_2) + 1}$

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