CMOS High Voltage Logic – CD4013B

Dual D-Type Flip-Flop Logic IC with Set and Reset in bare die form

Rev 1.0
21/11/17

Description

The CD4013B is fabricated using a 3µm 15CMOS process and consists of two identical, independent data type flip-flops. Each flip-flop has separate data, set, reset, clock inputs and Q,$\overline{Q}$ outputs. The device can be used in Shift Register applications and also Counter or Toggle applications by connecting Q output to the data input. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is clock independent and accomplished by a high level on the respective Set or Reset line.

Features:

- High Input Voltage up to 20V
- Symmetrical Output Characteristics
- Max input current 1µA at 18V over full Military Temperature Range
- Set-Reset Capability & Static Flip-Flop Operation
- Drives x2 Low–power TTL or x1 LSTTL Load
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

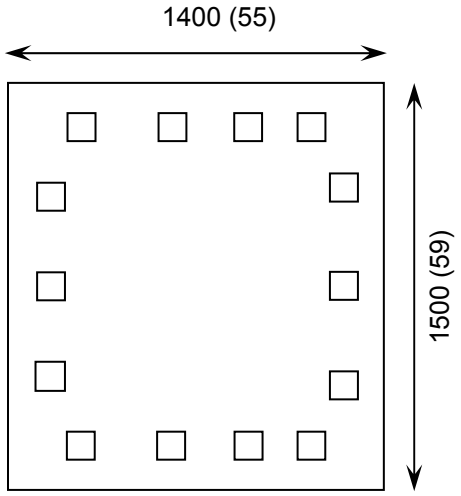
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1400 x 1500 55 x 59	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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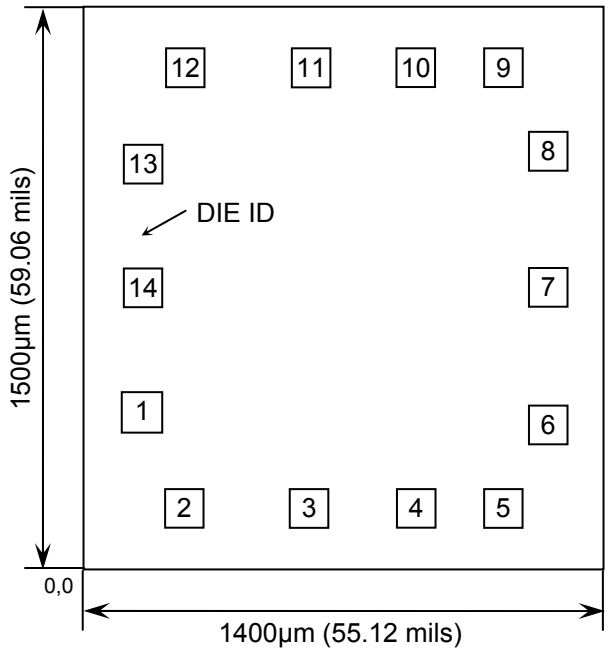
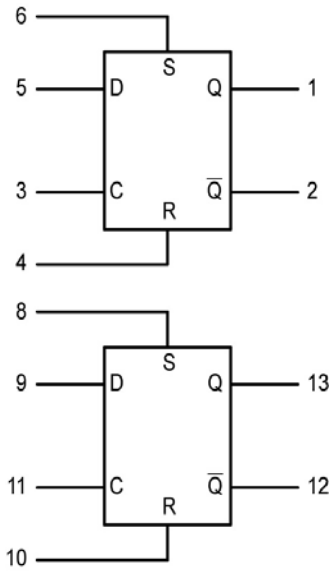
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	Q1	0.108	0.372
2	$\overline{Q}$1	0.222	0.113
3	CLOCK 1	0.550	0.113
4	RESET 1	0.833	0.113
5	D1	1.074	0.113
6	SET 1	1.191	0.338
7	V_{SS}	1.191	0.700
8	SET 2	1.191	1.062
9	D2	1.074	1.287
10	RESET 2	0.833	1.287
11	CLOCK 2	0.550	1.287
12	$\overline{Q}$2	0.222	1.287
13	Q2	0.108	1.028
14	V_{DD}	0.108	0.698
CONNECT CHIP BACK TO V_{DD} OR FLOAT			

Logic Diagram



V_{DD} = PAD 14
V_{SS} = PAD7

Truth Table

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⌐¯	0	0	0	0	1	
⌐¯	1	0	0	1	0	
¯⌐	X	0	0	Q	$\overline{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = DON'T CARE
† = LEVEL CHANGE

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Absolute Maximum Ratings[1]

PARAMETER		SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})		V_{DD}	-0.5 to +20	V
DC Input or Output Voltage (Referenced to V_{SS})		V_{IN}, V_{OUT}	-0.5 to V_{DD}+0.5	V
Storage Temperature Range		T_{STG}	-65 to 150	°C
Input Current or Output Current (per Pad)		I_{IN}, I_{OUT}	±10	mA
Power Dissipation in Still Air[2]	T_J = -55°C to 100°C	P_D	500	mW
	T_J = 100°C to 125°C		200	

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3.0	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of voltage higher than max rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Unused inputs must be tied to an appropriate logic voltage level (e.g. V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	5V	V_{OUT} =0.5V or V_{DD}= -0.5V	3.5	3.5	3.5	V
		10V	V_{OUT} =1.0V or V_{DD} =-1.0V	7	7	7	
		15V	V_{OUT} =1.5V or V_{DD} = -1.5V	11	11	11	
Maximum Low-Level Input Voltage	V_{IL}	5V	V_{OUT} =0.5V or V_{DD}= -0.5V	1.5	1.5	1.5	V
		10V	V_{OUT} =1.0V or V_{DD} =-1.0V	3	3	3	
		15V	V_{OUT} =1.5V or V_{DD} = 1.5V	4	4	4	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IN} = V_{SS} or V_{DD}	4.95	4.95	4.95	V
		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	

4. $-55^{\circ}C \le T_J \le +125^{\circ}C$

DC Electrical Characteristics Continued (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IL} = 1.5V, V_{IH} =3.5V, I_O = -1µA	4.5	4.5	4.5	V
		10V	V_{IL} = 3.0V, V_{IH} =7.0V, I_O = -1µA	9.0	9.0	9.0	
		15V	V_{IL} = 4.0V, V_{IH} =11.0V, I_O = -1µA	13.5	13.5	13.5	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IN} = V_{SS} or V_{DD}	0.05	0.05	0.05	V
		10V	V_{IN} = V_{SS} or V_{DD}	0.05	0.05	0.05	
		15V	V_{IN} = V_{SS} or V_{DD}	0.05	0.05	0.05	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IL} = 1.5V, V_{IH} =3.5V, I_O = 1µA	0.5	0.5	0.5	V
		10V	V_{IL} = 3.0V, V_{IH} =7.0V, I_O = 1µA	1.0	1.0	1.0	
		15V	V_{IL} = 4.0V, V_{IH} =11.0V, I_O = 1µA	1.5	1.5	1.5	
Maximum Input Leakage Current	I_{IN}	18V	V_{IN} = V_{SS} or V_{DD}	±0.1	±0.1	±1.0	µA
Maximum Quiescent Supply Current	I_{DD}	5V	V_{IN} = V_{SS} or V_{DD}	1	30	30	µA
		10V		2	60	60	
		15V		4	120	120	
		20V		20	600	600	
Minimum Output Low (Sink) Current	I_{OL}	5V	V_{IN} = V_{SS} or V_{DD}, V_{OL} = 0.4V	0.51	0.42	0.36	mA
		10V	V_{IN} = V_{SS} or V_{DD}, V_{OL} = 0.5V	1.3	1.1	0.9	
		15V	V_{IN} = V_{SS} or V_{DD}, V_{OL} = 1.5V	3.4	2.8	2.4	
Minimum Output High (Source) Current	I_{OH}	5V	V_{IN} = V_{SS} or V_{DD}, V_{OH} = 2.5V	-1.6	-1.3	-1.15	
		5V	V_{IN} = V_{SS} or V_{DD}, V_{OH} = 4.6V	-0.51	-0.42	-0.36	mA
		10V	V_{IN} = V_{SS} or V_{DD}, V_{OH} = 9.5V	-1.3	-1.1	-0.9	
		15V	V_{IN} = V_{SS} or V_{DD}, V_{OH} = 13.5V	-3.4	-2.8	-2.4	

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency	f_{max}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	3.5	3.5	3	MHz
		10V		8	8	6	
		15V		12	12	10	
Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1)	t_{PLH}, t_{PHL}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	300	300	450	ns
		10V		130	130	200	
		15V		90	90	150	
Propagation Delay, Set to Q or Reset to $\overline{Q}$ (Figure 2)	t_{PLH}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	300	300	450	ns
		10V		130	130	200	
		15V		90	90	150	
Propagation Delay, Set to $\overline{Q}$ or Reset to Q (Figure 2)	t_{PHL}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	400	400	600	ns
		10V		170	170	250	
		15V		120	120	150	
Output Transition Time, Any Output (Figure 1)	t_{TLH}, t_{THL}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	200	200	250	ns
		10V		100	100	150	
		15V		80	80	100	
Input Capacitance	C_{IN}	-	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	7.5	7.5	7.5	pF

Timing Requirements[5]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Pulse Width, Clock (Figure 1)	t_w	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	140	140	200	ns
		10V		60	60	80	
		15V		40	40	50	
Minimum Pulse Width, Set or Reset (Figure 2)	t_w	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	180	180	250	ns
		10V		80	80	120	
		15V		50	50	80	
Minimum Setup Time, Data to Clock	t_{su}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	40	40	40	ns
		10V		20	20	20	
		15V		15	15	15	
Minimum Hold Time, Clock to Data	t_h	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	5	5	8	ns
		10V		5	5	5	
		15V		5	5	5	
Maximum Input Rise or Fall Time, Clock (Figure 1)	t_r, t_f	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	500	500	500	ns
		10V		30	30	30	
		15V		6	6	6	

5. Not production tested in die form, characterized by chip design and tested in package.

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Switching Waveforms

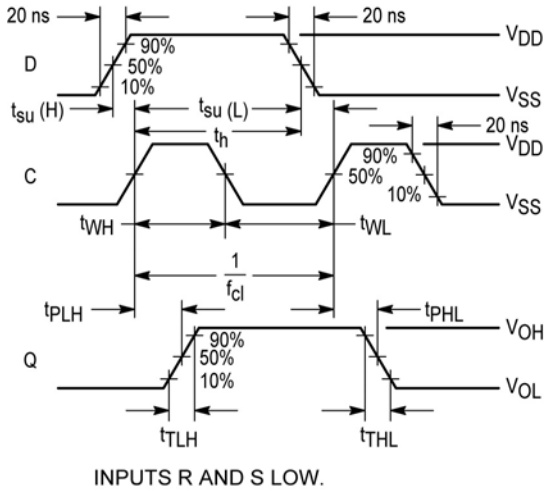

Figure 1 – Data, Clock and Output

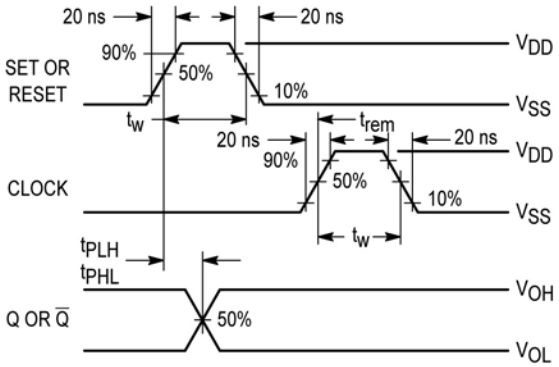

Figure 2 – Set, Reset, Clock and Output