



Low Voltage CMOS Logic – 74LVC1GU04

Single Unbuffered Inverter Gate in bare die form

Rev 1.1
03/09/20

Description

The 74LVC1GU04 single inverter gate performs the Boolean function $Y = \bar{A}$. The inverter can be driven by either 3.3V or 5V inputs enabling use of this device in a mixed 3.3V and 5V environment. The 74LVC1GU04 operates over a 1.65V to 5.5V supply range with low power consumption and is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing damaging backflow current through the device when it is powered down. The device finds use in oscillator and pulse shaping applications and as general purpose high-input impedance linear amplifier.

Features:

- Inputs accept up to 5.5V enabling level translation down to V_{CC}
- Wide Supply Voltage: V_{CC} 1.65V - 5.5V
- Output Drive capability: $\pm 24mA$, $V_{CC} = 3V$
- Low Quiescent Current: 10 μA max
- High speed: $t_{pd} < 5.0ns$, $V_{CC} = 3V$
- Unbuffered for stability in oscillator circuitry
- Tiny die size.

Ordering Information

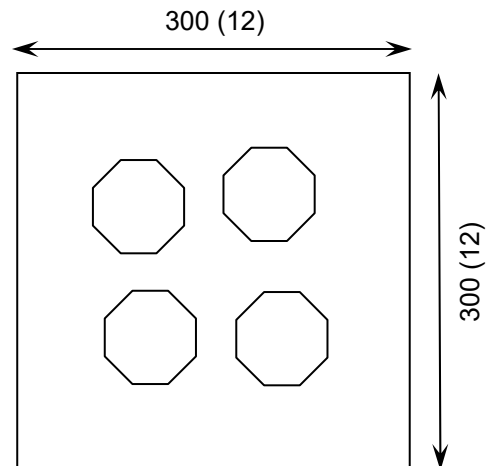
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54LVC1GU04](#)

Die Dimensions in μm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness \leftrightarrow 280 μm (11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	300 x 300 12 x 12	μm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	μm mils
Die Thickness	280 (± 20) 11.02 (± 0.79)	μm mils
Top Metal Composition	Al-Si-Cu 3 μm	
Back Metal Composition	N/A – Bare Si	

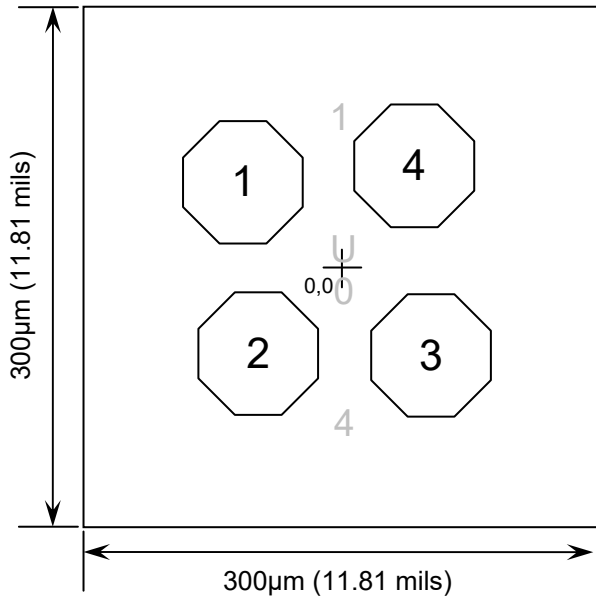




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Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	V _{CC}	-59	50
2	A	-50	-50
3	Y	50	-50
4	GND	41	59

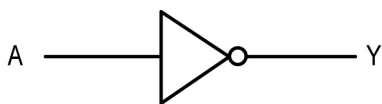
CONNECT CHIP BACK TO V_{CC} OR FLOAT

Function Table

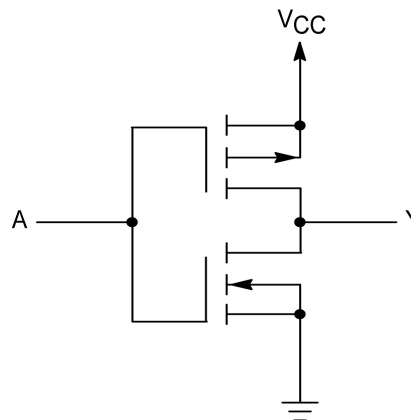
INPUT A	OUTPUT Y
H	L
L	H

H = High level (steady state)
L = Low level (steady state)

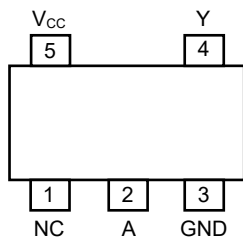
Logic Diagram



Expanded Logic Diagram



Pin Configuration in TSSOP5





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Absolute Maximum Ratings²

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +6.5	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to +6.5	V
DC Output Voltage – Active Mode	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage – Power-Down Mode $V_{CC} = 0V$		-0.5 to +5.5	V
DC Input Clamp Current, $V_{IN} < 0$	I_{IK}	-50	mA
DC Output Clamp Current, $V_{OUT} < 0$	I_{OK}	-50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} or GND Current	I_{CC}	± 100	mA
Power Dissipation in Still Air ³	P_D	250	mW
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 3. Measured in plastic TSSOP5 package, above 87.5°C the value of P_D derates linearly with 4.0 mW/K, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions⁴ (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	V_{CC}	1.65	5.5	V	
DC Supply Voltage – Data retention only	V_{CC}	1.5	-	V	
DC Input Voltage	V_{IN}	0	5.5	V	
DC Output Voltage	V_{OUT}	0	V_{CC}	V	
High-Level Output Current	I_{OH}	$V_{CC} = 1.65V$	-	-4	mA
		$V_{CC} = 2.3V$	-	-8	
		$V_{CC} = 2.7V$	-	-12	
		$V_{CC} = 3V$	-	-24	
		$V_{CC} = 4.5V$	-	-32	
Low-Level Output Current	I_{OL}	$V_{CC} = 1.65V$	-	4	mA
		$V_{CC} = 2.3V$	-	8	
		$V_{CC} = 2.7V$	-	12	
		$V_{CC} = 3V$	-	24	
		$V_{CC} = 4.5V$	-	32	
Operating Temperature Range	T_J	-40	+125	°C	
Input Transition Rise & Fall Rate	$\Delta t / \Delta V$	$V_{CC} = 1.65V - 2.7V$	0	20	ns/V
		$V_{CC} = 2.7V - 5.5V$	0	10	ns/V

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.





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DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Minimum High-Level Input Voltage	V _{IH}	1.65 - 1.95V	I _{OH} = -100µA	0.75 x V _{CC}	0.75 x V _{CC}	0.80 x V _{CC}	V
Maximum Low-Level Input Voltage	V _{IL}	1.65 - 1.95V	I _{OL} = -100µA	0.25 x V _{CC}	0.25 x V _{CC}	0.20 x V _{CC}	V
Minimum High-Level Output Voltage	V _{OH}	1.65 - 5.5V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = -100µA	V _{CC} - 0.1	V _{CC} - 0.1	V _{CC} - 0.1	V
		1.65V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = -4mA	1.2	1.2	0.95	
		2.3V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = -8mA	1.9	1.9	1.7	
		2.7V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = -12mA	2.2	2.2	1.9	V
		3.0V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = -24mA	2.3	2.3	2.0	
		4.5V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = -32mA	3.8	3.8	3.4	
Maximum Low-Level Output Voltage	V _{OL}	1.65 - 5.5V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 100µA	0.1	0.1	0.1	V
		1.65V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4mA	0.45	0.45	0.70	
		2.3V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 8mA	0.3	0.3	0.45	
		2.7V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 12mA	0.4	0.4	0.60	V
		3.0V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 24mA	0.55	0.55	0.80	
		4.5V	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 32mA	0.55	0.55	0.80	
Input Leakage Current	I _{IN}	0V - 5.5V	V _{IN} = 5.5V or GND	±1	±1	±5	µA
Power-Off Leakage Current	I _{OFF}	0V	V _{IN} or V _{OUT} = 5.5V	±2	±2	±2	µA
Supply Current	I _{CC}	1.65 - 5.5V	V _{IN} = 5.5V or GND, I _{OUT} = 0A	10	10	10	µA

5. -40°C ≤ T_J ≤ +125°C





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Dynamic Characteristics⁶

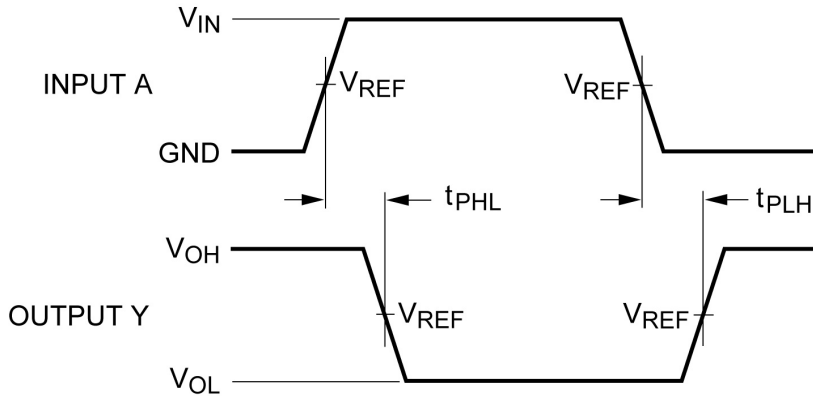
PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Propagation Delay Input A to Output Y (Figure 1,2)	t _{PD}	1.65 - 1.95V	C _L = 30pF, Input t _r = t _f ≤ 2ns, R _L = 1kΩ, V _{IN} = V _{CC}	5.0	5.5	6.5	ns
		2.3 - 2.7V	C _L = 30pF, Input t _r = t _f ≤ 2ns, R _L = 500Ω, V _{IN} = V _{CC}	4.0	4.5	5.5	
		2.7V	C _L = 50pF, Input t _r = t _f ≤ 2.5ns, R _L = 500Ω, V _{IN} = 2.7V	4.5	5.0	6.5	
		3.0 - 3.6V	C _L = 50pF, Input t _r = t _f ≤ 2.5ns, R _L = 500Ω, V _{IN} = 3V	3.7	4.2	5.0	
		4.5 - 5.5V	C _L = 50pF, Input t _r = t _f ≤ 2.5ns, R _L = 500Ω, V _{IN} = V _{CC}	3.0	3.5	4.0	
Input Capacitance	C _{IN}	3.3V	V _{IN} = GND to V _{CC} , T _J = 25°C	TYPICAL 7			pF
Power Dissipation Capacitance ⁷	C _{PD}	3.3V	V _{IN} = GND to V _{CC} , T _J = 25°C	TYPICAL 13			pF

6. Not production tested in die form, characterized by chip design and tested in package. 7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ in microwatts.





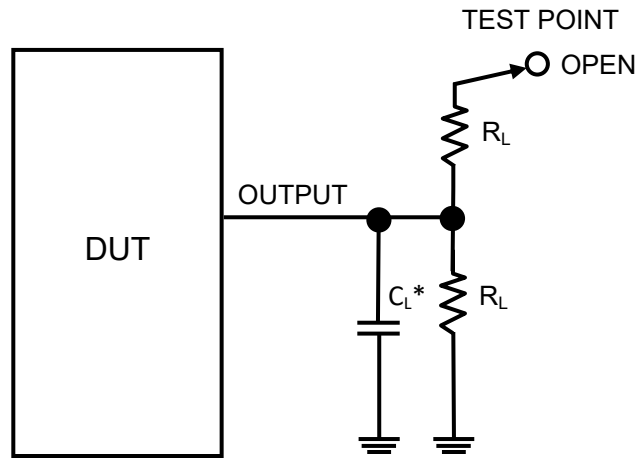
Switching Waveform



MEASUREMENT POINTS		
V_{CC}	V_{IN}	V_{REF}
1.65 - 1.95V	V_{CC}	$0.5 \times V_{CC}$
2.3 - 2.7V	V_{CC}	$0.5 \times V_{CC}$
2.7V	2.7V	1.5V
3.0 - 3.6V	2.7V	1.5V
4.5 - 5.5V	V_{CC}	$0.5 \times V_{CC}$

Figure 1 – Propagation Delay Input to Output

Test Circuit



* Includes all probe and jig capacitance

Figure 2 – Test Setup

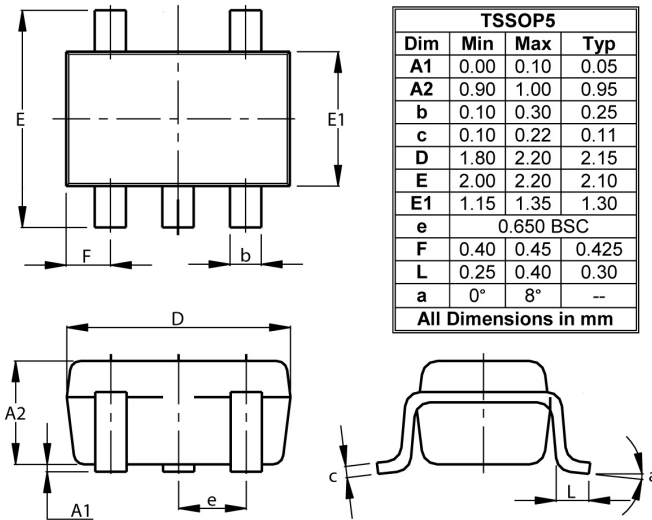




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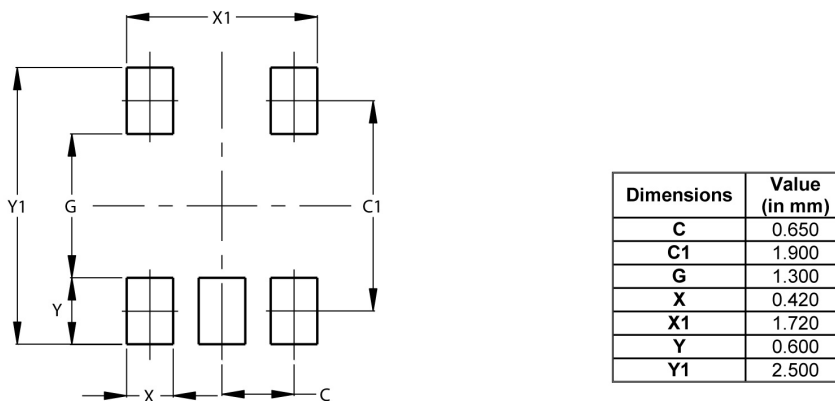
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Package Drawing – TSSOP5



- Surface Mount Package
- Weight: 0.006 grams (approximately)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020
- Case Material – Molded Plastic, UL Flammability Rating 94V-0
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)

Suggested Package Layout – TSSOP5



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