Low Power Schottky Logic – 74LS138

3-to-8 Line Decoder / Demultiplexer IC in bare die form

Rev 1.0
21/11/17

Description

The 74LS138 3-to-8 Line Decoder / Demultiplexer is fabricated on a 2µm 40V Bipolar process. The device decodes 1-of-8 lines, set by x3 binary select inputs & three enable inputs. Multiple Input Enables allow parallel expansion to a 24-line decoder using x3 74LS138 devices or a 32 line decoder using x4 74LS138 + inverter. The LS138 can be used as an 8-output demultiplexer by using one active LOW Enable input as data input & the other Enable inputs as strobes. Unused Enable inputs must be permanently tied to their appropriate active HIGH or active LOW state.

Features:

- Demultiplexing capability
- Multiple Input Enables for parallel expansion
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

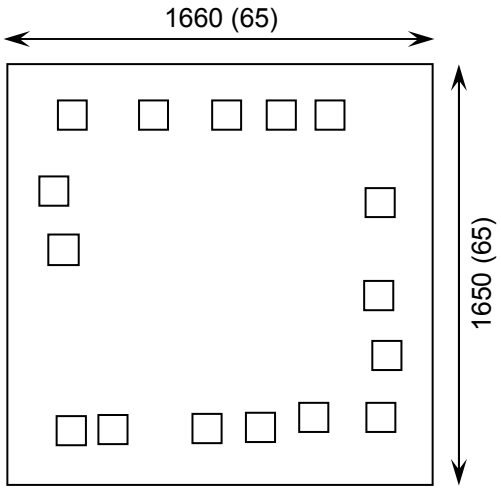
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54LS138

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Plastic Package – On request

Mechanical Specification

Die Size (Unsawn)	1660 x 1650 65 x 65	µm mils
Minimum Bond Pad Size	116 x 116 4.57 x 4.57	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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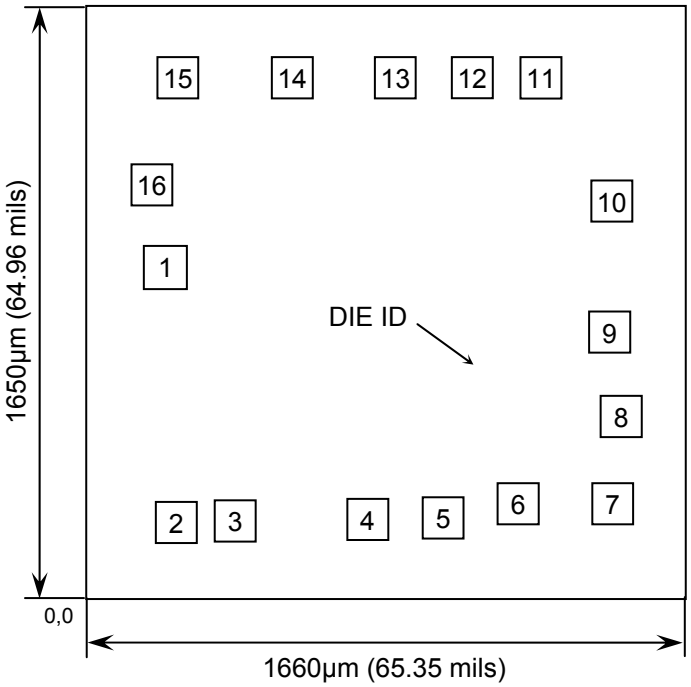
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A	0.173	0.875
2	B	0.197	0.169
3	C	0.361	0.171
4	$\overline{G}$2A	0.725	0.176
5	$\overline{G}$2B	0.929	0.184
6	G1	1.141	0.220
7	Y7	1.405	0.221
8	GND	1.425	0.461
9	Y6	1.393	0.695
10	Y5	1.398	1.054
11	Y4	1.198	1.395
12	Y3	1.022	1.395
13	Y2	0.804	1.395
14	Y1	0.524	1.395
15	Y0	0.202	1.395
16	V_{CC}	0.135	1.099
CONNECT CHIP BACK TO GND OR FLOAT			

Truth Table

INPUTS						OUTPUTS							
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High level (steady state)
L = Low level (steady state)
X = Don't care

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{CC}	7.0	V
DC Input Voltage	V_{IN}	7.0	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.75	5.25	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
High-Level Output Current	I_{OH}	-	-0.4	mA
Low-Level Output Current	I_{OL}	-	8	mA
Operating Temperature Range	T_J	-40	+85	°C

DC Electrical Characteristics[2] T_J = -40°C to 85°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage	V_{IK}	V_{CC} = MIN I_{IN} = -18mA	-	-0.65	-1.5	V
Output Voltage High	V_{OH}	V_{CC} = MIN, I_{OH} = MAX V_{IN} = V_{IL} or V_{IH} per Function Table	2.7	3.5	-	V
Output Voltage Low	V_{OL}	V_{CC} = MIN I_{OH} = MAX V_{IN} = V_{IL} or V_{IH} per Truth Table; I_{OL} = 8mA	-	0.35	0.5	V
Input High Current	I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V	-	-	20	µA
		V_{CC} = MAX, V_{IN} = 7.0V	-	-	0.1	mA
Input Low Current	I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V	-	-	-0.4	mA
Short Circuit Current[3]	I_{OS}	V_{CC} = MAX	-20	-	-100	mA
Power Supply Current (Total)	I_{CC}	V_{CC} = MAX	-	6.3	10	mA

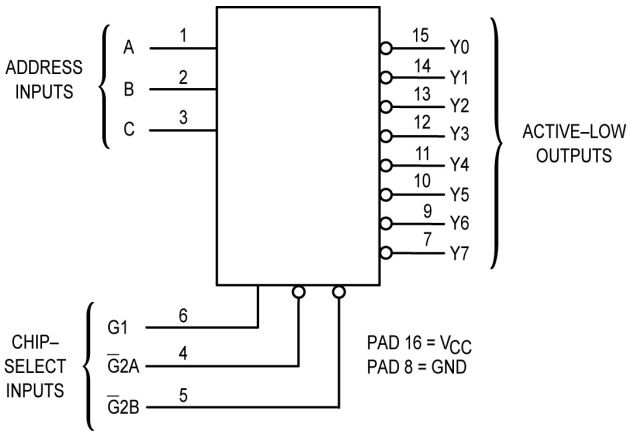
2. All typical values @ V_{CC} = 5V, T_J = 25°C. **3.** Not more than one output should be shorted at a time, nor for more than 1 second.

AC Electrical Characteristics[4]

PARAMETER	SYMBOL	CONDITIONS	DELAY LEVELS	LIMITS			UNITS
				MIN	TYP	MAX	
Propagation Delay, Address to Output	t_{PLH}	V_{CC} = 5V, C_L = 15pF	2	-	13	20	ns
	t_{PHL}		2	-	27	41	
Propagation Delay, Other Input High	t_{PLH}	V_{CC} = 5V, C_L = 15pF	3	-	18	27	ns
	t_{PHL}		3	-	26	39	
Propagation Delay, $\overline{G}$2B or G2A Enable to Output	t_{PLH}	V_{CC} = 5V, C_L = 15pF	2	-	12	18	ns
	t_{PHL}		2	-	21	32	
Propagation Delay, G1 Enable to Output	t_{PLH}	V_{CC} = 5V, C_L = 15pF	3	-	17	26	ns
	t_{PHL}		3	-	25	38	

4. Not production tested in die form, characterized by chip design and tested in package .

Logic Diagram



Switching Waveforms