High Speed CMOS Logic – 74HC595

8-bit shift registers with 3-state output latches in bare die form

Rev 1.2
22/12/21

Description

The 74HC595 is an 8–bit serial-in to parallel-out shift register which drives an 8–bit D–type latch with 3–state outputs. Both register and latch have independent positive triggered clock inputs. All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together the input shift register is always one clock cycle ahead of the output register. The shift register also features asynchronous reset. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS595.

Ordering Information

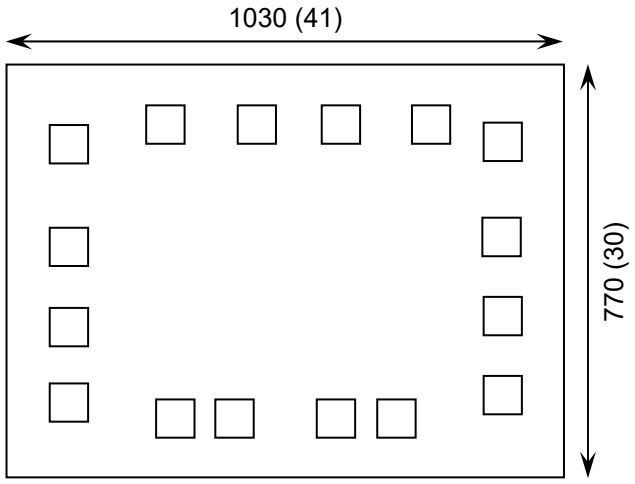
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC595

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1030 x 770 41 x 30	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±10) 11.02 (±0.39)	µm mils
Top Metal Composition	Al-Si-Cu 2.8 µm	
Back Metal Composition	N/A – Bare Si	

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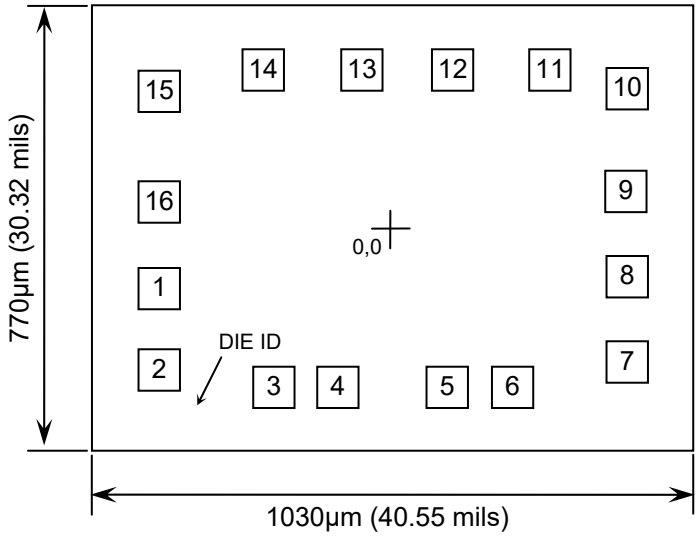
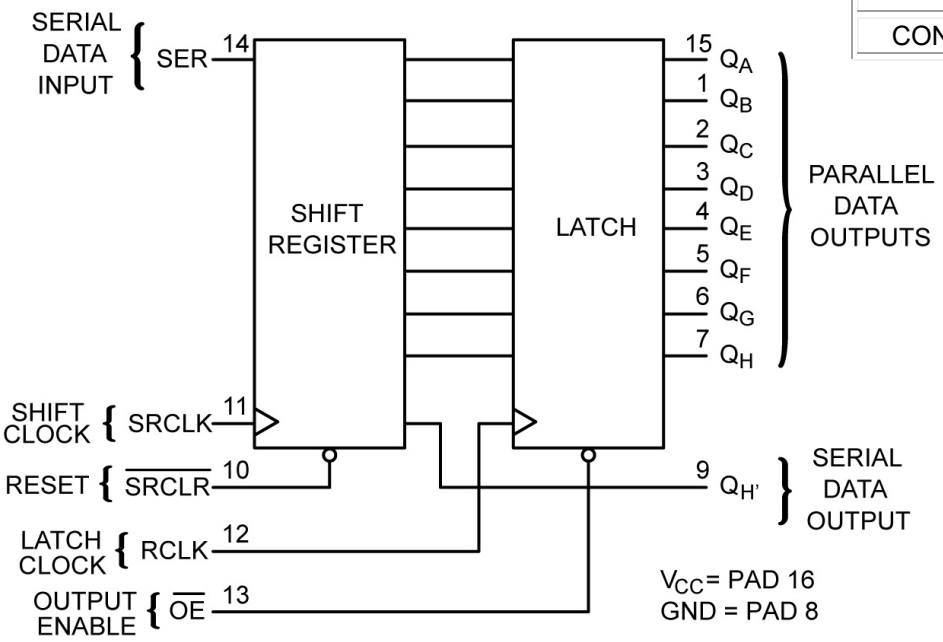
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	Q_B	-401.8	-102
2	Q_C	-401.8	-246
3	Q_D	-205.8	-273
4	Q_E	-95.8	-273
5	Q_F	95.8	-273
6	Q_G	205.8	-273
7	Q_H	401.8	-230.2
8	GND	401.8	-84.6
9	$Q_{H'}$	401.8	62.6
10	$\overline{SRCLR}$	401.8	243.2
11	SRCLK	272	273
12	RCLK	103.2	273
13	$\overline{OE}$	-54.4	273
14	SER	-233.2	273
15	Q_A	-401.8	237.6
16	V_{CC}	-401.8	46
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



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Function Table[1]

INPUTS					OUTPUTS		FUNCTION
SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	$Q_{H'}$	Q_N	
X	X	L	L	X	L	NC	LOW level on $\overline{SRCLR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift-register loaded into storage register
X	X	H	L	X	L	Z	Shift-register clear. Parallel outputs in high- impedance OFF-state
↑	X	L	H	H	$Q_{G'}$	NC	Logic high level shifted into shift register stage 0. Content of all shift register stages shifted through, e.g. previous state of stage 6 (internal $Q_{6'}$) appears on serial output($Q_{H'}$)
X	↑	L	H	X	NC	Qn'	Contents of shift register stages (internal Qn') transfers to the storage register and parallel output stages
↑	↑	L	H	X	$Q_{G'}$	Qn'	Shift register contents shifted through. Previous shift register content transfers to storage register & parallel output stages.

1. H=HIGH voltage level; L=LOW voltage level; ↑ =LOW-to-HIGH transition; Z=high-impedance OFF-state; NC=no change; X=don't care.

Absolute Maximum Ratings[2]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±35	mA
DC V_{CC} or GND Current	I_{CC}	±75	mA
Power Dissipation in Still Air[3]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **3.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[4] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-40	+85	°C
Input Rise or Fall Times	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	ns
	V_{CC} = 6.0V		0	400	ns

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	
Minimum High-Level Output Voltage (Q_A – Q_H)	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 2.4mA$	2.48	2.34	2.34	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0mA$	3.98	3.84	3.84	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 7.8mA$	5.48	5.34	5.34	
Maximum Low-Level Output Voltage (Q_A–Q_H)	V_{OL}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 2.4mA$	0.26	0.33	0.33	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0mA$	0.26	0.33	0.33	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 7.8mA$	0.26	0.33	0.33	
Minimum High-Level Output Voltage ($Q_{H'}$)	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 2.4mA$	2.48	2.34	2.34	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0mA$	3.98	3.84	3.84	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 5.2mA$	5.48	5.34	5.34	

5. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Low-Level Output Voltage ($Q_{H'}$)	V_{OL}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 2.4mA$	0.26	0.33	0.33	V
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 4.0mA$	0.26	0.33	0.33	
		6.0V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \leq 5.2mA$	0.26	0.33	0.33	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Three-State Leakage Current (Q_A–Q_H)	I_{OZ}	6.0V	High-Impedance Output State, $V_{IN} = V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND	±0.5	±5.0	±5.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	4	40	40	µA

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Clock Frequency (50% Duty Cycle) (Figure 1,7)	f_{max}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	6.0	4.8	4.8	MHz
		3.0V		15	10	10	
		4.5V		30	24	24	
		6.0V		35	28	28	
Maximum Propagation Delay, SRCLK to $Q_{H'}$ (Figure 1,7)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	140	175	175	ns
		3.0V		100	125	125	
		4.5V		28	35	35	
		6.0V		24	30	30	
Maximum Propagation Delay, $\overline{SRCLR}$ to $Q_{H'}$ (Figure 2,7)	t_{PHL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	145	180	180	ns
		3.0V		100	125	125	
		4.5V		29	36	36	
		6.0V		25	31	31	
Maximum Propagation Delay, RCLK to Q_A – Q_H (Figure 3,7)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	140	175	175	ns
		3.0V		100	125	125	
		4.5V		28	35	35	
		6.0V		24	30	30	

6. Not production tested in die form, characterized by chip design and tested in package.

AC Electrical Characteristics continued[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Propagation Delay, $\overline{OE}$ to $Q_A - Q_H$ (Figure 4,8)	t_{PLZ}, t_{PHZ}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	150	190	190	ns
		3.0V		100	125	125	
		4.5V		30	38	38	
		6.0V		26	33	33	
Maximum Propagation Delay, $\overline{OE}$ to $Q_A - Q_H$ (Figure 4,8)	t_{PZL}, t_{PZH}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	135	170	170	ns
		3.0V		90	110	110	
		4.5V		27	34	34	
		6.0V		23	29	29	
Maximum Output Transition Time, $Q_A - Q_H$ (Figure 3,7)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	60	75	75	ns
		3.0V		23	27	27	
		4.5V		12	15	15	
		6.0V		10	13	13	
Maximum Output Transition Time, $Q_{H'}$ (Figure 1,7)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, Input $t_r = t_f$ = 6ns	75	95	95	ns
		3.0V		27	32	32	
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Maximum Three-State Output Capacitance, $Q_A - Q_H$	C_{OUT}	-	High-Impedance Output State	15	15	15	pF
Power Dissipation Capacitance[7]	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				300			

7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum Setup Time, SER to SRCLK (Figure 5)	t_{su}	2.0V	Input $t_r = t_f$ = 6ns	50	65	65	ns
		3.0V		40	50	50	
		4.5V		10	13	13	
		6.0V		9	11	11	
Minimum Setup Time, SRCLK to RCLK (Figure 6)	t_{su}	2.0V	Input $t_r = t_f$ = 6ns	75	95	95	ns
		3.0V		60	70	70	
		4.5V		15	19	19	
		6.0V		13	16	16	

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum Hold Time, SRCLK to SER (Figure 5)	t_h	2.0V	Input $t_r = t_f = 6ns$	5	5	5	ns
		3.0V		5	5	5	
		4.5V		5	5	5	
		6.0V		5	5	5	
Minimum Recovery Time, $\overline{\text{SRCLR}}$ to SRCLK (Figure 2)	t_{rec}	2.0V	Input $t_r = t_f = 6ns$	50	65	65	ns
		3.0V		40	50	50	
		4.5V		10	13	13	
		6.0V		9	11	11	
Minimum Pulse Width, $\overline{\text{SRCLR}}$ (Figure 2)	t_w	2.0V	Input $t_r = t_f = 6ns$	60	75	75	ns
		3.0V		45	60	60	
		4.5V		12	15	15	
		6.0V		10	13	13	
Minimum Pulse Width, SRCLK (Figure 1)	t_w	2.0V	Input $t_r = t_f = 6ns$	50	65	65	ns
		3.0V		40	50	50	
		4.5V		10	13	13	
		6.0V		9	11	11	
Minimum Pulse Width, RCLK (Figure 6)	t_w	2.0V	Input $t_r = t_f = 6ns$	50	65	65	ns
		3.0V		40	50	50	
		4.5V		10	13	13	
		6.0V		9	11	11	
Maximum Input Rise and Fall Times, (Figure 1)	t_r, t_f	2.0V	Input $t_r = t_f = 6ns$	1000	1000	1000	ns
		3.0V		800	800	800	
		4.5V		500	500	500	
		6.0V		400	400	400	

Switching Waveforms

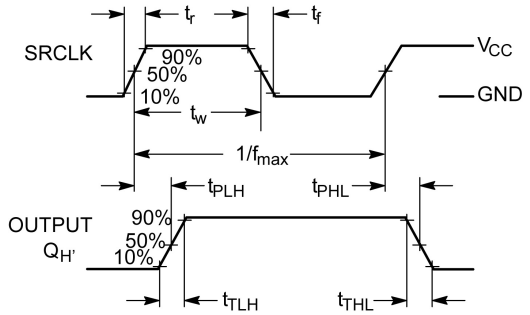


Figure 1 – Clock Propagation Delay & Output Timing

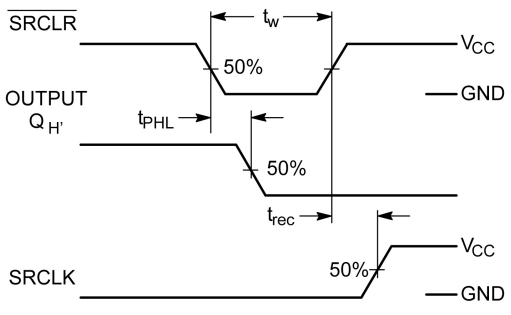


Figure 2 – Reset Propagation Delay & Timing

Switching Waveforms continued

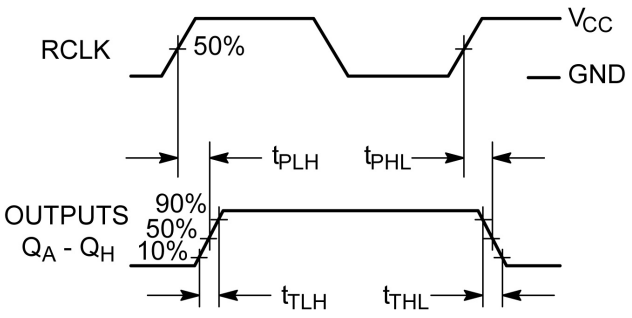


Figure 3 – Clock Propagation Delay & Output Timing

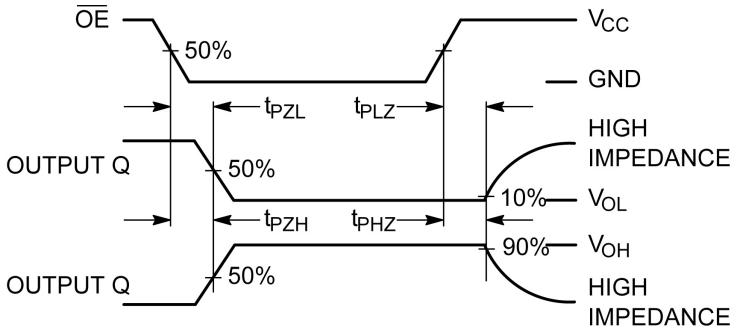


Figure 4 – Enable to Output Propagation Delay

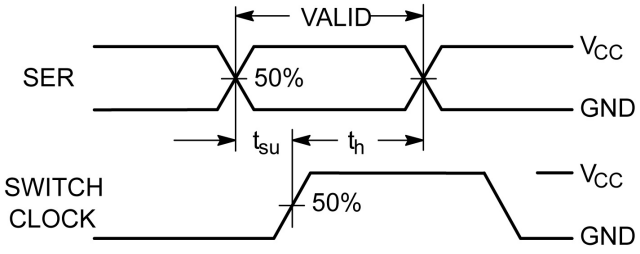


Figure 5 – Data Transition Timing, Serial Input & Clock

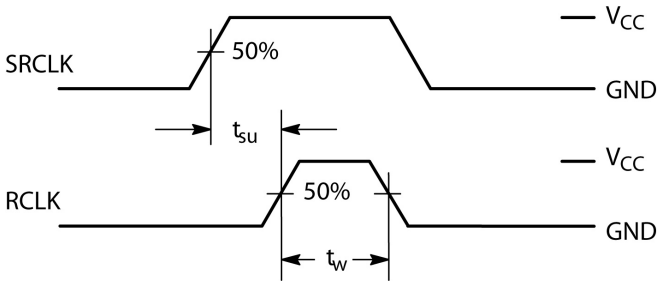
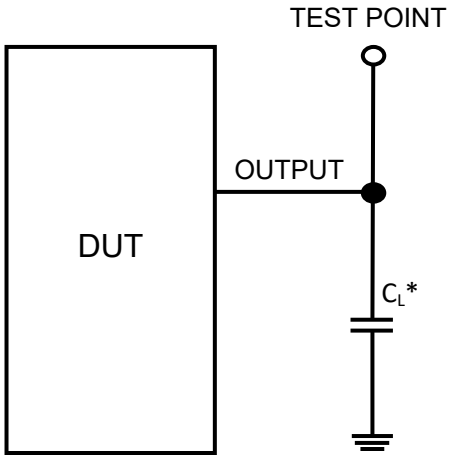
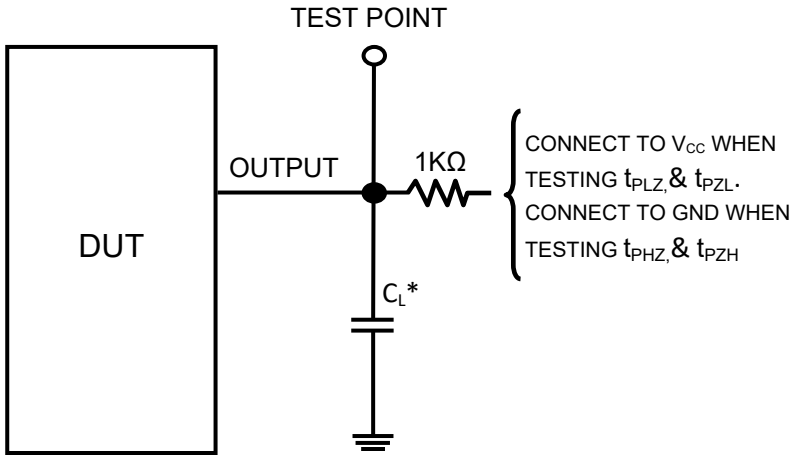


Figure 6 – Shift Clock to Register Clock Setup Timing



* Includes all probe and jig capacitance

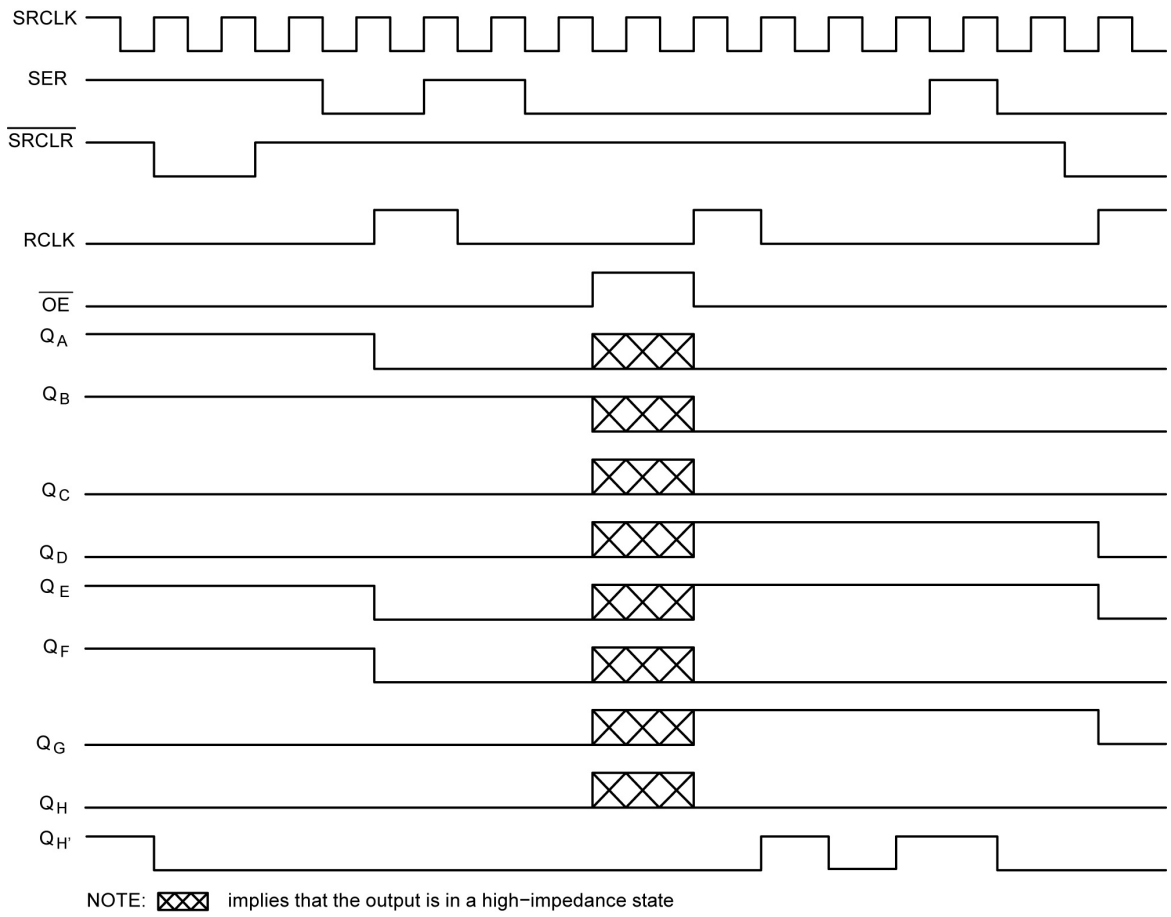
Figure 7 – Test Setup



* Includes all probe and jig capacitance

Figure 8 – Test Setup

Timing Diagram



NOTE: ⊠ implies that the output is in a high−impedance state