High Speed CMOS Logic – 74HC27

Triple 3-Input NOR Gate in bare die form

Rev 1.0
22/04/19

Description

The 74HC27 triple 3-Input NOR Gate is fabricated on a 2.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power The device contains three independent 3-input NOR gates performing Boolean function $Y = (\overline{A + B + C})$ or $Y = \overline{A} \cdot \overline{B} \cdot \overline{C}$ in positive logic. Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- Function compatible with 54LS27
- High Noise Immunity CMOS process.

Ordering Information

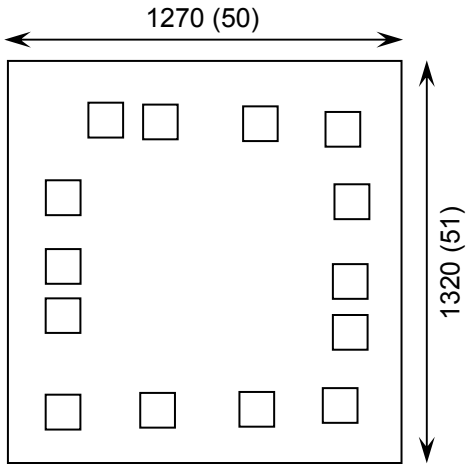
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC27

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1270 x 1320 50 x 51	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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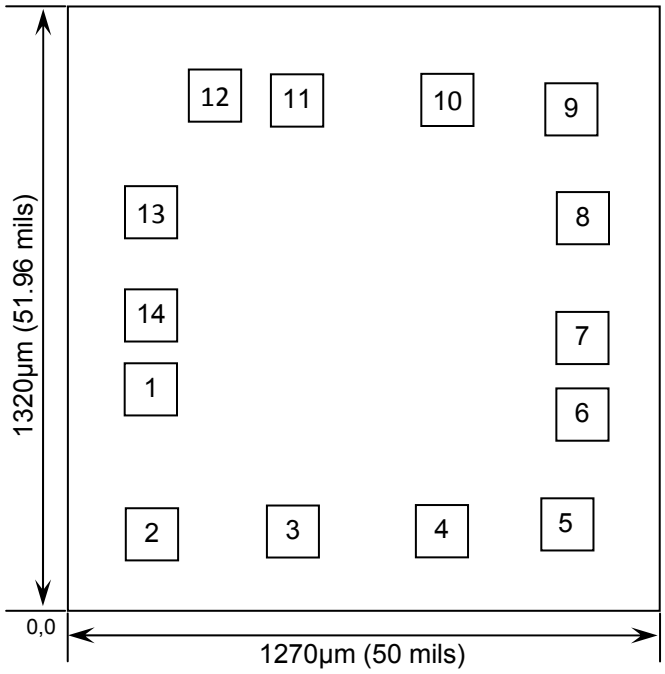
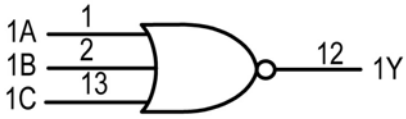
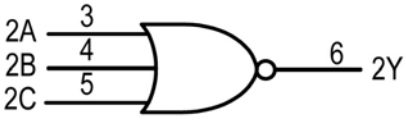
Pad Layout and Functions



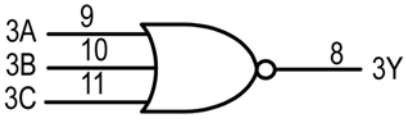
PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.129	0.442
2	1B	0.132	0.124
3	2A	0.433	0.133
4	2B	0.751	0.133
5	2C	1.017	0.148
6	2Y	1.047	0.392
7	GND	1.047	0.561
8	3Y	1.047	0.828
9	3A	1.017	1.073
10	3B	0.751	1.088
11	3C	0.433	1.088
12	1Y	0.262	1.095
13	1C	0.128	0.838
14	V_{CC}	0.129	0.606
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram





$Y = \overline{A + B + C}$



Pad 14 = V_{CC}
Pad 7 = GND

Truth Table

INPUTS			OUTPUT
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = High level (steady state)
L = Low level (steady state)
X = don't care

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-40	+85	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6.0V	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 4.0mA$	3.98	3.84	3.84	
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 5.2mA$	5.48	5.34	5.34	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IL}$ or V_{IL} $\|I_{OUT}\| \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IL}$ or V_{IL} $\|I_{OUT}\| \leq 4.0mA$	0.26	0.33	0.33	
		6.0V	$V_{IN} = V_{IL}$ or V_{IL} $\|I_{OUT}\| \leq 5.2mA$	0.26	0.33	0.33	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	2	20	20	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Input A, B or C to Output Y (Figure 1,2)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	90	115	115	ns
		4.5V		18	23	23	
		6.0V		15	20	20	
Maximum Output Rise and Fall Time, Any Output (Figure 1,2)	t_{TLH}, t_{THL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	75	95	95	ns
		4.5V		15	19	19	
		6.0V		13	16	16	

5. Not production tested in die form, characterized by chip design and tested in package.

AC Electrical Characteristics Continued[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[6]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				27			

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

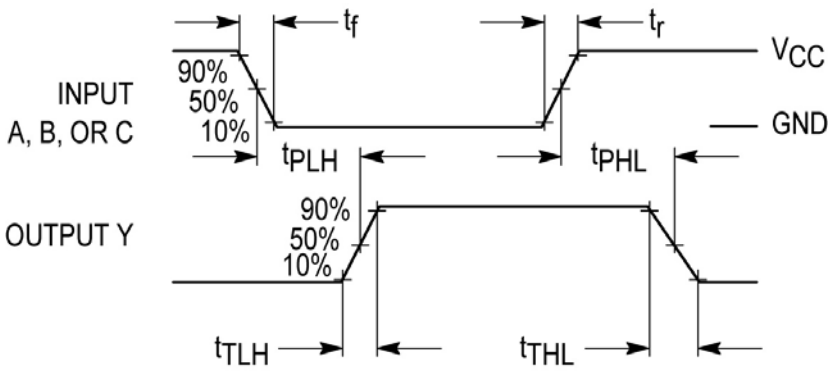
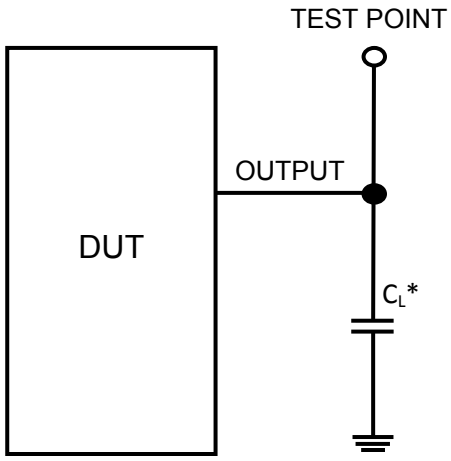


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



* Includes all probe and jig capacitance

Figure 2

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