High Speed CMOS Logic – 74HC109

Dual J-K Flip-flop with Set and Reset in bare die form

Rev 1.0
16/4/18

Description

The 74HC109 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. The J and K logic level at positive clock edge changes the devices output state. Set and Reset functions are asynchronous, operating independently of the clock and executed by a logic low on the corresponding input. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS109.

Ordering Information

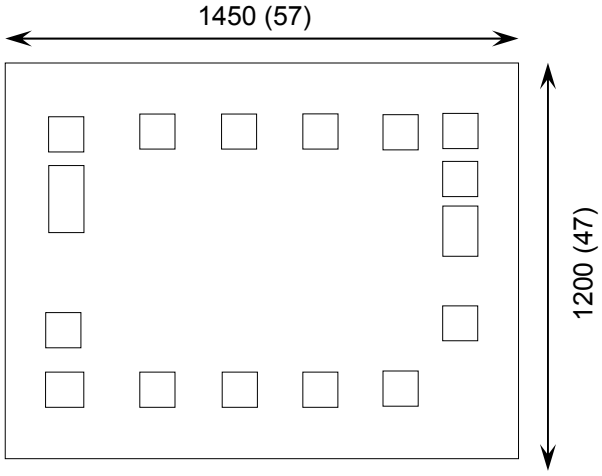
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC109

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1450 x 1200 57 x 47	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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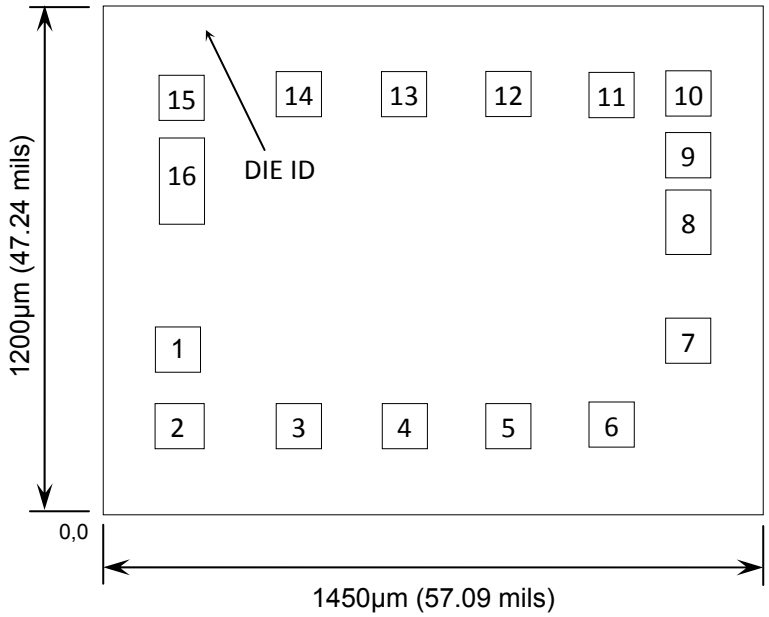
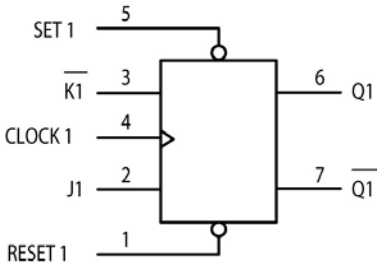
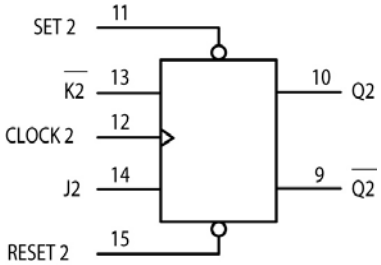
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	RESET 1	0.130	0.375
2	J1	0.140	0.135
3	$\overline{K1}$	0.395	0.145
4	CLOCK 1	0.625	0.145
5	SET 1	0.850	0.145
6	Q1	1.035	0.165
7	$\overline{Q1}$	1.220	0.420
8	GND	1.230	0.700
9	$\overline{Q2}$	1.230	0.890
10	Q2	1.220	0.935
11	SET 2	1.045	0.935
12	CLOCK 2	0.815	0.935
13	$\overline{K2}$	0.585	0.935
14	J2	0.360	0.935
15	RESET 2	0.130	0.900
16	V_{CC}	0.120	0.605
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram





Pad 16 = V_{CC}
Pad 8 = GND

Truth Table

INPUTS					OUTPUTS	
SET	RESET	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	NO CHANGE	
H	H	↓	H	H	H	L
H	H	L	X	X	NO CHANGE	

* Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±25	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	0	+85	°C
Input Rise and Fall Time	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	

4. 0°C ≤ T_J ≤ +85°C

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 4.0mA$	0.26	0.33	0.40	
		6.0V	$V_{IN} = V_{IL}$ $\lvert I_{OUT} \rvert \leq 5.2mA$	0.26	0.33	0.40	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	80	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency (50% Duty Cycle) (Figure 1,4)	f_{max}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	6.0	4.8	4.0	MHz
		4.5V		30	24	20	
		6.0V		35	28	24	
Maximum Propagation Delay, Clock to Q or Q (Figure 1,4)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	175	220	265	ns
		4.5V		35	44	53	
		6.0V		30	37	45	
Maximum Propagation Delay, Set or Reset to Q or Q (Figure 2,4)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	230	290	345	ns
		4.5V		46	58	69	
		6.0V		39	49	59	
Maximum Output Rise and Fall Time (Figure 1,4)	t_{TLH}, t_{THL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	75	95	110	ns
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance (Per Flip-Flop)[6]	C_{PD}	-	$T_J = 25°C$, $V_{CC} = 5.0V$	TYPICAL			pF
				40			

5. Not production tested in die form, characterized by chip design and tested in packagE.

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, J or K to Clock (Figure 3)	t_{su}	2.0V	Input $t_r = t_f = 6ns$	100	125	150	ns
		4.5V		20	25	30	
		6.0V		17	21	26	
Minimum Hold Time, Clock to J or K (Figure 3)	t_h	2.0V	Input $t_r = t_f = 6ns$	5	5	5	ns
		4.5V		5	5	5	
		6.0V		5	5	5	
Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	t_{rec}	2.0V	Input $t_r = t_f = 6ns$	5	5	5	ns
		4.5V		5	5	5	
		6.0V		5	5	5	
Minimum Pulse Width, Set or Reset (Figure 2)	t_w	2.0V	Input $t_r = t_f = 6ns$	80	100	120	ns
		4.5V		16	20	24	
		6.0V		14	17	20	
Minimum Pulse Width, Clock (Figure 2)	t_w	2.0V	Input $t_r = t_f = 6ns$	80	100	120	ns
		4.5V		16	20	24	
		6.0V		14	17	20	
Maximum Input Rise and Fall Times (Figure 1)	t_r, t_f	2.0V	Input $t_r = t_f = 6ns$	1000	1000	1000	ns
		4.5V		500	500	500	
		6.0V		400	400	400	

Switching Waveforms

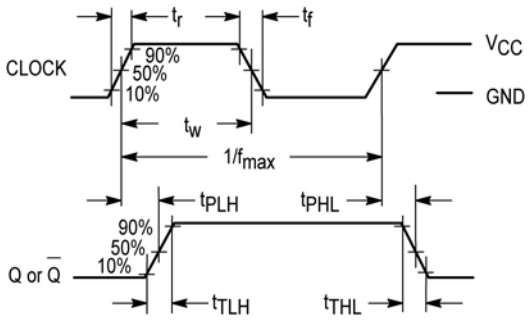


Figure 1

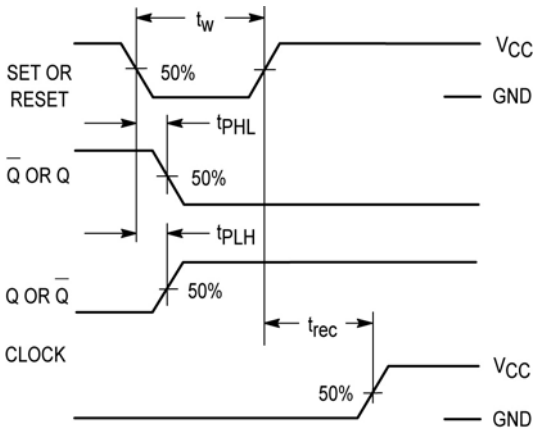


Figure 2

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Switching Waveforms

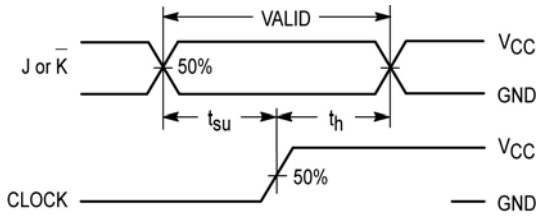
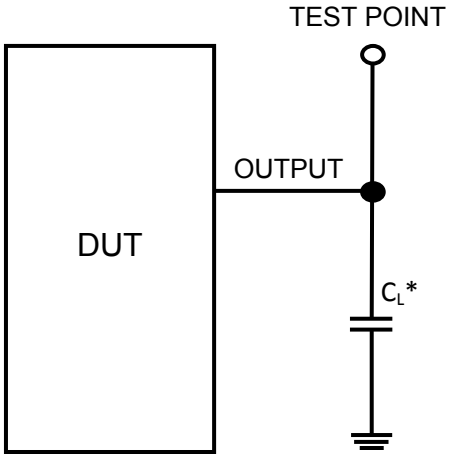


Figure 3

Test Circuit



* Includes all probe and jig capacitance

Figure 4