

Quad 2-Input NOR Gates in bare die form

Rev 1.0 22/04/19

Description

The 74HC02 2-Input NOR Gate is fabricated on a .35µm advanced CMOS process combining high speed LSTTL performance with CMOS low power. The device performs the Boolean function Y = $(\overline{A} + \overline{B})$ or Y = $\overline{A} \cdot \overline{B}$ in positive logic. Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. The product die size is significantly smaller than industry peers due to its re-design and production using a more advanced CMOS process.

Features:

Output Drive Capability: 10 LSTTL Loads

■ Low Input Current: 1µA

Outputs directly interface CMOS, NMOS and TTL

Operating Voltage Range: 2V to 6V

Function compatible with 54LS02

High Noise Immunity CMOS process.

Ordering Information

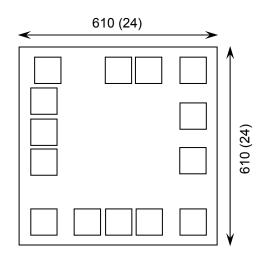
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC02

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

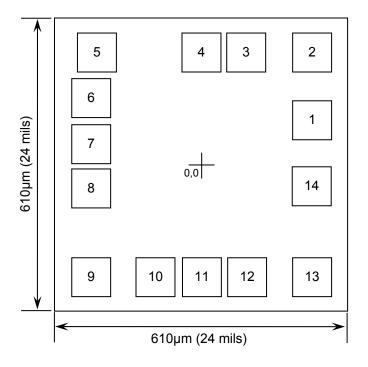
Die Size (Unsawn)	610 x 610 24 x 24	μm mils
Minimum Bond Pad Size	85 x 85 3.35 x 3.35	μm mils
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils
Top Metal Composition	Al 1%Si 1.1μ	m
Back Metal Composition	N/A – Bare S	Si



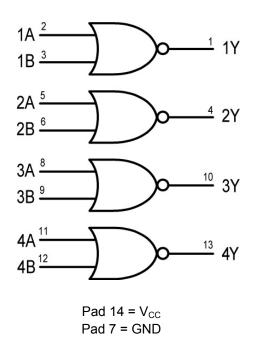


Rev 1.0 22/04/19

Pad Layout and Functions



Logic Diagram



PAD	FUNCTION	COORDIN	ATES (µm)
PAD	FUNCTION	X	Υ
1	1Y	230	95
2	1A	230	230
3	1B	95	230
4	2Y	0	230
5 6	2A	-220	230
	2B	-230	140
7	GND	-230	45
8	3A -230		-52
9	3B	-230	-230
10	3Y	-95	-230
11	4A	0	-230
12	4B	95	-230
13	4Y	230	-230
14	V _{CC}	230	-45
CON	NECT CHIP BA	CK TO V _{CC} C	R FLOAT

Truth Table

INPL	JTS	OUTPUT
Α	В	Υ
L L H	L H L H	H L L
	_	el (steady state)





Rev 1.0 22/04/19

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-0.5 to V _{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
DC Input Current	I _{IN}	±20	mA
DC Output Current, per pad	I _{OUT}	±25	mA
DC Supply Current, V _{CC} or GND	I _{CC}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V _{CC}		2	6	V
DC Input or Output Voltage	V _{IN} ,V _{OUT}		0	V _{CC}	V
Operating Temperature Range	T _J		0	+85	°C
	t _r , t _f	V _{CC} = 2V	0	1000	
Input Rise or Fall Times		$V_{CC} = 4.5V$	0	500	ns
		V _{CC} = 6.0V	0	400	

^{3.} This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc} CON	CONDITIONS		LIMITS		
	OTHIBOL	V CC	CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS
Minimum High-Level Input Voltage		2.0V	., .,	1.5	1.5	1.5	
	V _{IH}	3.0V	V _{OUT} = 0.1V or V _{CC} -0.1V I _{OUT} ≤ 20μA	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
		2.0V		0.5	0.5	0.5	
Maximum Low-Level Input Voltage	V _{IL}	3.0V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	0.9	0.9	0.9	V
	VIL	4.5V	V _{CC} -0.1V I _{OUT} ≤ 20μA	1.35	1.35	1.35	V
		6.0V	1-0011	1.8	1.8	1.8	

^{4.} $0^{\circ}C \le T_{J} \le +85^{\circ}C$





Rev 1.0 22/04/19

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIM	ITS	UNITS
TANAMETER	STINIDOL	▼ CC	CONDITIONS	25°C	85°C	FULL RANGE⁴	Civilo
		2.0V	\/ =\/ or\/	1.9	1.9	1.9	V
		4.5V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 20 \mu A$	4.4	4.4	4.4	
		6.0V	1.0011 = 1	5.9	5.9	5.9	
Minimum High-Level Output Voltage	V _{OH}	3.0V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 2.4 \text{mA}$	2.48	2.34	2.34	
3		4.5V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	3.98	3.84	3.84	V
		6.0V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	5.48	5.34	5.34	
		2.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $ I_{OUT} \le 20 \mu A $	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V	1.0011	0.1	0.1	0.1	
Maximum Low-Level Output Voltage	V _{OL}	3.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 2.4 \text{mA}$	0.26	0.33	0.33	
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	0.26	0.33	0.33	V
		6.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	0.26	0.33	0.33	
Maximum Input Leakage Current	I _{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current	I _{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	1	10	10	μА

AC Electrical Characteristics⁵

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		UNITS		
	OTHIBOL	₩66	CONDITIONS	25°C	85°C	FULL RANGE⁴	ONTO
Maximum Propagation Delay, Input A or B to Output Y	to H to H	2.0V		75	95	95	
		3.0V	$C_L = 50pF,$ $t_r = t_f = 6ns$	30	40	40	ns
		4.5V		15	19	19	
(Figure 1,2)		6.0V		13	16	16	
Maximum Output Rise	ne 3.0	2.0V	C _L = 50pF,	75	95	95	
and Fall Time, Any Output (Figure 1,2)		3.0V		30	40	40	ns
	t _{TLH} , t _{THL}	4.5V	$t_r = t_f = 6$ ns	15	19	19	115
		6.0V		13	16	16	

 $[\]textbf{5.} \ \ \text{Not production tested in die form, characterized by chip design and tested in package}.$





AC Electrical Characteristics Continued⁵

Rev 1.0 22/04/19

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIM	ITS	UNITS
	OTHEOL	• 66	CONDITIONS	25°C	85°C	FULL RANGE⁴	Oitilo
Maximum Input Capacitance	C _{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate ⁶	C _{PD}	-	$T_A = 25^{\circ}C,$ $V_{CC} = 5.0V$		TYPI		pF

^{6.} Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

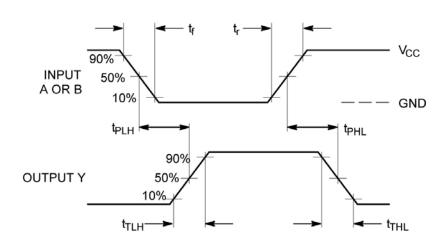
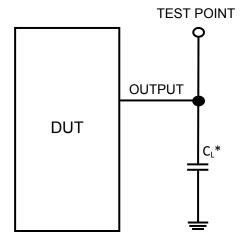


Figure 1 - Propagation Delay & Output Transition Time

Test Circuit



^{*} Includes all probe and jig capacitance

Figure 2

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

