

4-bit Binary Counter Logic IC in bare die form

Rev 1.1 28/08/21

Description

The 74ALS93 4-bit binary counter is fabricated using a 2µm 40V bipolar process. The device comprises two 4-bit ripple type counters consisting of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has independent clock (CK) & asynchronous master reset (R0) inputs. Counter state change is triggered by a high-to-low transition on the clock. Each section can be used separately or tied together (Q to CK) to form BCD or modulo-16 counters.

Features:

- Low Power Consumption
- Input Clamp Diodes Limit High Speed Termination Effects
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

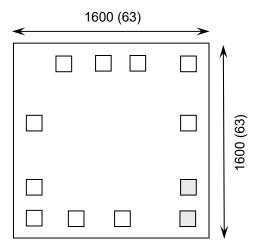
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ALS93

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

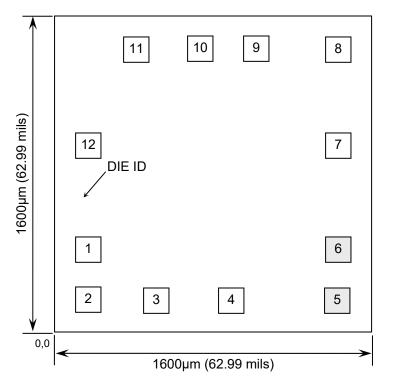
Die Size (Unsawn)	1600 x 1600 63 x 63	μm mils	
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	μm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils	
Top Metal Composition	Metal Composition Al 1%Si 1.1µm		
Back Metal Composition	N/A – Bare Si		





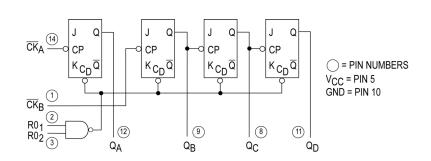
Rev 1.1 28/08/21

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (m		
FAD	FUNCTION	X	Y	
1	CK _B	0.100	0.360	
2	R0 ₍₁₎	0.100	0.100	
3	R0 ₍₂₎	0.450	0.100	
4	V _{CC}	0.830	0.100	
5	NC	1.370	0.100	
6	NC	1.370	0.360	
7	Q _C	1.370	0.880	
8	Q_B	1.370	1.370	
9	GND	0.960	1.370	
10	Q_D	0.670	1.370	
11	Q_A	0.350	1.370	
12	CKA	0.100	0.880	
CONNECT CHIP BACK TO GND				

Logic Diagram



Mode Selection

RESET INPUT		OUTPUT				
R0 ₍₁₎	R0 ₍₂₎	Q_A	Q_B	Q_{C}	Q_D	
Н	Н	L	L	L	L	
L	Н	COUNT				
Н	L	COUNT				
L	L	COUNT				

Truth Table

COUNT		OUTPUT				
000111	Q_A	Q_B	Q _C	Q_D		
0	L	L	L	L		
1	Н	L	L	L		
2	L	Н	L	L		
3	Н	Н	L	L		
4	L	L	H	L		
5	Н	L	H	L		
6	L	Н	Н	L		
7	H	Н	H	L		
8	L	L	L	Н		
9	Н	L	L	Н		
10	L	Н	L	Н		
11	H	Н	L	Н		
12	L	L	H	Н		
13	Н	L	H	Н		
14	L	Н	H	Н		
15	Н	Н	Н	Н		
NOTE: OUTPUT	Q _A IS CO	NNECTED	TO INPU	Т СКв		

NOTE: OUTPUT Q_A IS CONNECTED TO INPUT CK_B

H = HIGH Voltage Level
L = LOW Voltage Level





Rev 1.1 28/08/21

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	7.0	V
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

DADAMETED OVADOL MIN MAY LINITO								
PARAMETER	SYMBOL	MIN	MAX	UNITS				
Supply Voltage (Referenced to GND)	V _{CC}	4.75	5.25	V				
High-Level Input Voltage	V _{IH}	2	-	V				
Low-Level Input Voltage	V _{IL}	-	0.8	V				
High-Level Output Current	I _{OH}	-	-0.4	mA				
Low-Level Output Current	I _{OL}	-	8	mA				
Operating Temperature Range	TJ	-40	+85	°C				

DC Electrical Characteristics Voltages referenced to GND, T_J = -40°C to 85°C unless otherwise specified

PARAMETER	SYMBOL CONDITIONS		LIMITS			
		MIN	TYP	MAX	UNITS	
Minimum High-Level Input Voltage	V _{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V _{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage	V _{IK}	$V_{CC} = 4.5V$ $I_{IN} = -18mA$	-	-0.65	-1.5	V
Output Voltage High	V _{OH}	$V_{CC} = 4.5V, I_{OH} = -0.4mA$	V _{CC} -2	-	-	V
Output Voltage Low	V _{OL}	$V_{CC} = 4.5V$, $I_{OL} = 4mA$	-	0.25	0.4	V
	VOL	$V_{CC} = 4.5V, I_{OL} = 8mA$	-	0.35	0.5	
Input High Current	1	$V_{CC} = 5.5V, V_{IN} = 2.7V$	-	-	20	μA
Input High Current	I _{IH}	$V_{CC} = 5.5V, V_{IN} = 7.0V$	-	-	0.1	mA
Input Low Current	I _{IL}	$V_{CC} = 5.5V, V_{IL} = 0.4V$	-	-	-0.1	mA
Short Circuit Current ²	I _{OS}	$V_{CC} = 5.5V, V_{OUT} = 2.25V$	-30	-	-112	mA
Supply Current	I _{CC}	$V_{CC} = 5.5V$	-	-	13	mA

^{2.} Not more than one output should be shorted at a time, nor for more than 1 second.





AC Electrical Characteristics 4 V_{CC} = 5V, T_J = -40°C to 85°C unless otherwise specified

Rev 1.1 28/08/21

PARAMETER	SYMBOL CONDITIONS			LIMITS			
IANAMETER	STRIBOL	IIIBOL GONDINONO	MIN	TYP	MAX	UNITS	
Input Clock Frequency, CK _A	- f _{max}		32	-	-	MHz	
Input Clock Frequency, CK _B	max	$C_L = 50 pF, R_L = 510 \Omega$	16	-	-	MHz	
Fall, Rising Edge	t _f , t _r		-	-	2	ns	
Propagation Delay, CK_A to Q_A	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	16	ns	
Propagation Delay, CK_A to Q_A	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	18	115	
Propagation Delay, CK_A to Q_D	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	70	ns	
Propagation Delay, CK_A to Q_D	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	70	ns	
Propagation Delay, CK_B to Q_B	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	16	ns	
Propagation Delay, CK_B to Q_B	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	21	ns	
Propagation Delay, CK_B to Q_C	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	32	ns	
Propagation Delay, CK_B to Q_C	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	35	ns	
Propagation Delay, CK_B to Q_D	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	51	ns	
Propagation Delay, CK_B to Q_D	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	51	ns	
Propagation Delay, R0 to any output	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	32	ns	

Timing Requirements 4 V_{CC} = 5V, T_J = -40°C to 85°C unless otherwise specified

PARAMETER	SYMBOL CONDITIONS	LIMITS			UNITS	
TAKAMETEK		GONDITIONS	MIN	TYP	MAX	Oillio
CK _A Pulse Width	t _w	$C_L = 50 pF, R_L = 510 \Omega$	15	-	-	ns
CK _B Pulse Width			30	-	-	ns
R0 Pulse Width			15	-	-	ns
Recovery Time, R0 to CK	t _{REC}	$C_L = 50 pF, R_L = 510 \Omega$	25	-	-	ns

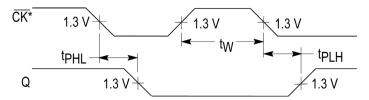
^{4.} Not production tested in die form, characterized by chip design.



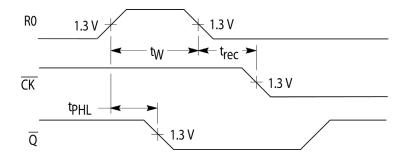


Rev 1.1 28/08/21

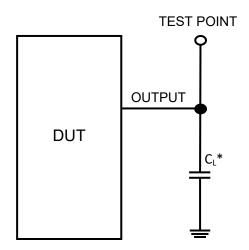
Switching Waveforms



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.



Test Circuit



* Includes all probe and jig capacitance

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

* Includes all probe and jig capacitance LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

