Advanced Low Power Schottky Logic - 74ALS174

Hex D-type Flip-Flop in bare die form

Description

The 74ALS174 Hex D-type Flip-Flop is fabricated using a 2µm 40V Bipolar process. The device is comprised of six flip-flops each having independent data input and data output. Load and clear is simultaneous, triggered by common clock and master reset respectively. D-Input levels transfer to Q output with the positive clock pulse.

Features:

- High speed 2ns (Min) propagation delay
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

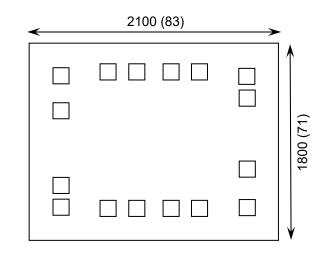
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ALS174

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

Die Size (Unsawn)	2100 x 1800 83 x 71	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µ	m
Back Metal Composition	N/A – Bare S	Si



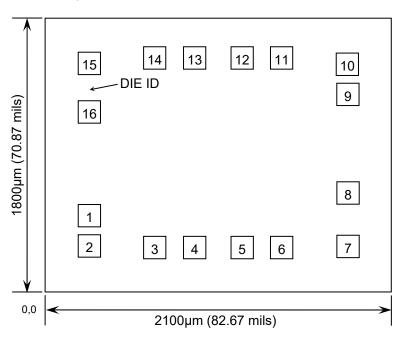
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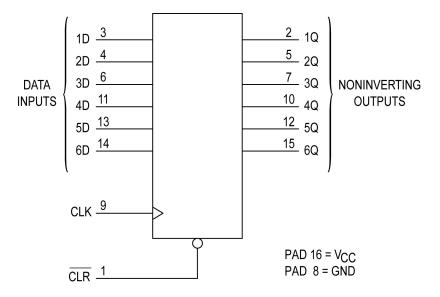


Pad Layout and Functions

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Logic Diagram



PAD	FUNCTION	COORDIN	ATES (mm)				
	1 ONO HON	X	Y				
1	CLR	0.200	0.435				
2	1Q	0.200	0.240				
3	1D	0.600	0.200				
4	2D	0.840	0.200				
5	2Q	1.130	0.200				
6	3D	1.370	0.200				
7	3Q	1.770	0.240				
8	GND	1.770	0.590				
9	CLK	1.770	1.240				
10	4Q	1.770	1.435				
11	4D	1.370	1.470				
12	5Q	1.130	1.470				
13	5D	0.840	1.470				
14	6D	0.600	1.470				
15	6Q	0.200	1.435				
16	V _{cc}	0.200	1.120				
	CONNECT CHIP BACK TO GND						

Function Table

INPUTS			OUTPUT			
CLR	CLK	D	Q			
L	Х	Х	L			
Н		Н	Н			
Н		L	L			
Н	L	Х	Q0			
H = High level (steady state)						
L = Low level (steady state)						
<pre>_/ = Low-to-High clock transition</pre>						
X = Don't care						



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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V _{CC}	7.0	V
DC Input Voltage	V _{IN}	7.0	V
Storage Temperature Range	T _{STG}	-65 to 150	C°

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{CC}	4.5	5.5	V
High-Level Input Voltage	V _{IH}	2	-	V
Low-Level Input Voltage	V _{IL}	-	0.8	V
High-Level Output Current	I _{ОН}	-	-0.4	mA
Low-Level Output Current	I _{OL}	-	8	mA
Operating Temperature Range	TJ	-40	+55	°C

DC Electrical Characteristics² $T_J = -40^{\circ}C$ to 85°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS		LIMITS		UNITS
FARAMETER	STWIDOL	CONDITIONS	MIN	TYP	MAX	
Minimum High-Level Input Voltage	V _{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V _{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage	VIK	$V_{CC} = MIN$ $I_{IN} = -18mA$	-	-	-1.5	V
Output Voltage High	V _{OH}	V _{CC} = 4.5V to 5.5V, I _{OH} = -0.4mA	V _{cc} -2	-	-	V
Output Voltage Low	V _{OL}	V _{CC} = 4.5V I _{OL} = 8mA	-	0.35	0.5	V
Input Current	I _{IN}	V_{CC} = 5.5V, V_{IN} = 7V	-	-	0.1	mA
Input High Current	I _{IH}	V_{CC} = 5.5V, V_{IN} = 2.7V	-	-	20	μA
Input Low Current	IL	$V_{CC} = 5.5, V_{IN} = 0.4V$	-	-	-0.1	mA
Output Current ³	Ι _Ο	V_{CC} = 5.5, V_{OUT} = 2.25V	-20	-	-112	mA
Power Supply Current (Total)	I _{CC}	$V_{\rm CC}$ = 5.5V , $V_{\rm IN}$ = 4.5V	-	11	19	mA

2. All typical values @ V_{CC} = 5V, T_J = 25°C.

3. Output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios



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AC Electrical Characteristics⁴ $T_J = -40^{\circ}C$ to 85°C unless otherwise specified

PARAMETER	SYMBOL		CONDITIONS	LIMITS			UNITS	
	OTMEOL	VCC	CONDITIONO	MIN	TYP	MAX		
Maximum Clock Frequency	f _{max}	5V ±10%	C _L = 50pF, R _L = 500Ω	50	-	-	MHz	
Maximum Propagation Delay, CLR to Q (Figure 1)	t _{PLH,}	5V ±10% C _L = 50pF, R _L = 500Ω			5	-	18	ns
	t _{PHL}		8	-	23			
Maximum Propagation Delay, CLK to Q (Figure 1)	t _{PLH,}	5V ±10%	C _L = 50pF,	3	-	15	ns	
	t _{PHL}	01 10/0	R _L = 500Ω	5	-	17		

Timing Requirements⁴ $T_J = -40^{\circ}C$ to 85°C unless otherwise specified

PARAMETER	PARAMETER SYMBOL V _{cc} CONDITIONS	Vac	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX			
Minimum Pulse Width, CLK (Figure 3)	$t_{w(H),}t_{w(L),}$	5V ±10%	$C_L = 50 pF,$ $R_L = 500 \Omega$	10	-	-	ns
Minimum Pulse Width, CLR (Figure 3)	t _{w(L)}	5V ±10%	$C_L = 50 pF,$ $R_L = 500 \Omega$	10	-	-	ns
Minimum Setup Time Before CLK (Figure 2)	t _{su}	5V ±10%	Data, C _L = 50pF, R _L = 500Ω	10	-	-	ns
Minimum Setup Time Before CLK (Figure 2)	t _{su}	5V ±10%	$\overline{\text{CLR}} \text{ Inactive,} \\ \text{C}_{L} = 50 \text{pF,} \\ \text{R}_{L} = 500 \Omega$	6	-	-	ns
Hold Time, Data after CLK (Figure 2)	t _h	5V ±10%	$C_L = 50 pF,$ $R_L = 500 \Omega s$	0	-	-	ns

4. Not production tested in die form, characterized by chip design and tested in package.



Switching Waveform

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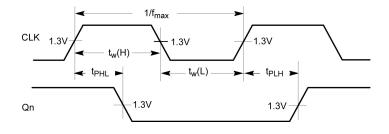
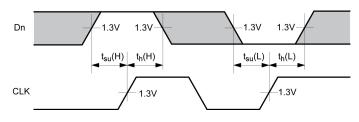
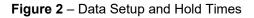


Figure 1 – Propagation Delay Clock to Output and minimum Clock Frequency





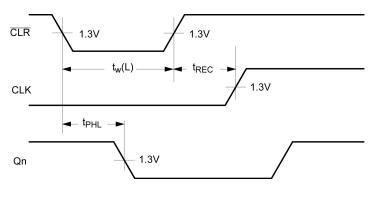
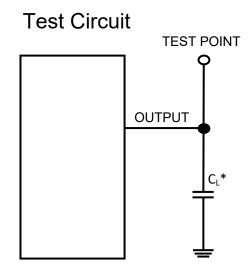


Figure 3 – Reset to Output, Reset to Clock Recovery



* Includes all probe and jig capacitance

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