Advanced High Speed CMOS Logic - 74AHC595

8-bit shift registers with 3-state output latches in bare die form

Rev 1.0
26/02/26

Description

The 74AHC595 is an 8–bit serial-in to parallel-out shift register which drives an 8–bit D–type latch with 3–state outputs. Both register and latch have independent positive triggered clock inputs. All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together the input shift register is always one clock cycle ahead of the output register. The shift register also features asynchronous reset. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Features:

- High Frequency: 110 MHz (Min) V_{CC} = 5V, C_L = 15pF
- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 0.1µA
- Outputs directly interface CMOS, NMOS and TTL
- CMOS High Noise Immunity
- Function compatible with 74LS595
- Performance upgrade for 74AC595, 74HC595
- Extended Industrial Temperature Range.

Ordering Information

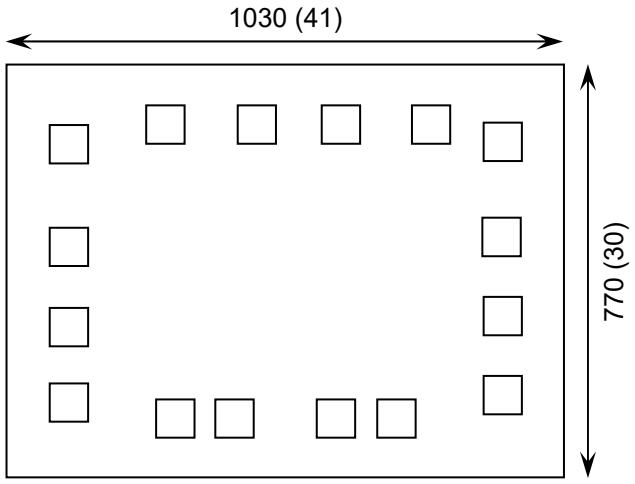
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54AHC595

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1030 x 770 41 x 30	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±10) 11.02 (±0.39)	µm mils
Top Metal Composition	Al-Si-Cu 2.8 µm	
Back Metal Composition	N/A – Bare Si	

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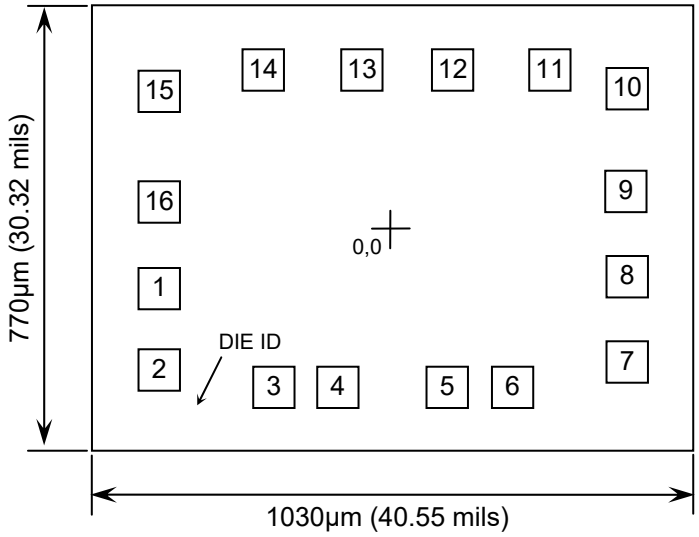
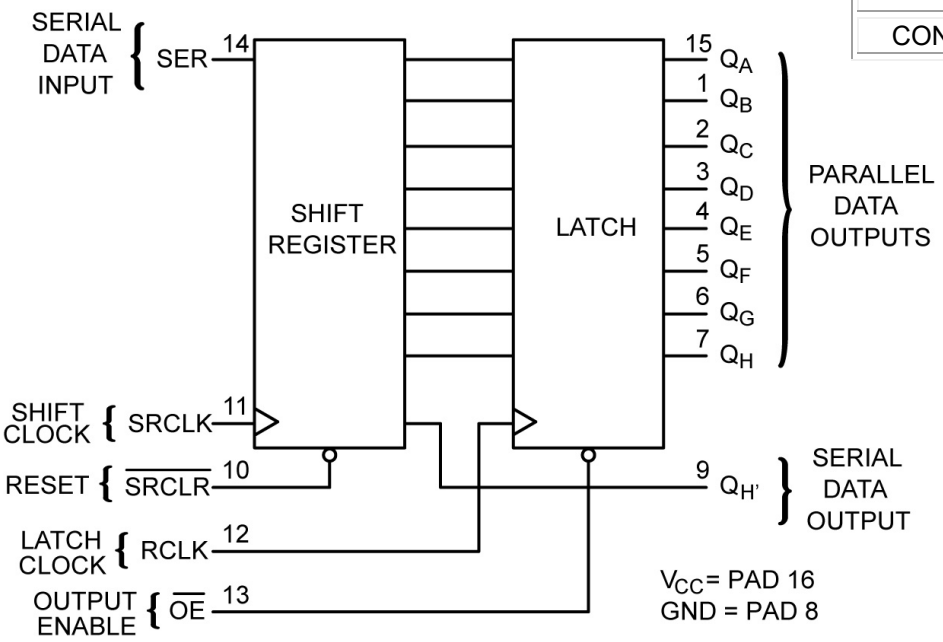
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	Q_B	-401.8	-102
2	Q_C	-401.8	-246
3	Q_D	-205.8	-273
4	Q_E	-95.8	-273
5	Q_F	95.8	-273
6	Q_G	205.8	-273
7	Q_H	401.8	-230.2
8	GND	401.8	-84.6
9	$Q_{H'}$	401.8	62.6
10	$\overline{SRCLR}$	401.8	243.2
11	SRCLK	272	273
12	RCLK	103.2	273
13	$\overline{OE}$	-54.4	273
14	SER	-233.2	273
15	Q_A	-401.8	237.6
16	V_{CC}	-401.8	46
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



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Function Table[1]

INPUTS					OUTPUTS		FUNCTION
SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	$Q_{H'}$	Q_N	
X	X	L	L	X	L	NC	LOW level on $\overline{SRCLR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift-register loaded into storage register
X	X	H	L	X	L	Z	Shift-register clear. Parallel outputs in high- impedance OFF-state
↑	X	L	H	H	$Q_{G'}$	NC	Logic high level shifted into shift register stage 0. Content of all shift register stages shifted through, e.g. previous state of stage 6 (internal $Q_{6'}$) appears on serial output($Q_{H'}$)
X	↑	L	H	X	NC	Qn'	Contents of shift register stages (internal Qn') transfers to the storage register and parallel output stages
↑	↑	L	H	X	$Q_{G'}$	Qn'	Shift register contents shifted through. Previous shift register content transfers to storage register & parallel output stages.

1. H=HIGH voltage level; L=LOW voltage level; ↑ =LOW-to-HIGH transition; Z=high-impedance OFF-state; NC=no change; X=don't care.

Absolute Maximum Ratings[2]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to +7.0	V
DC Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC V_{CC} or GND Current	I_{CC}	±75	mA
Power Dissipation in Still Air[3]	P_D	500	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **3.** Measured in plastic SOP-16 package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[4] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	5.5	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-40	+85	°C
Input Transition Rise or Fall Rate	V_{CC} = 3.3V ± 0.3V	Δt/Δv	0	100	ns/V
	V_{CC} = 5V ± 0.5V		0	20	ns/V

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \le 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		5.5V		1.65	1.65	1.65	
Minimum High-Level Output Voltage	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 50\mu A$	1.9	1.9	1.9	V
		3.0V		2.9	2.9	2.9	
		4.5V		4.4	4.4	4.4	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4mA$	2.58	2.48	2.48	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 8mA$	3.94	3.80	3.80	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 50\mu A$	0.1	0.1	0.1	V
		3.0V		0.1	0.1	0.1	
		4.5V		0.1	0.1	0.1	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4mA$	0.36	0.44	0.44	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 8mA$	0.36	0.44	0.44	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum Three-State Leakage Current	I_{OZ}	5.5V	High-Impedance Output State, V_{IN} = V_{IH} or V_{IL}, V_{OUT}=V_{CC} or GND	±0.25	±2.5	±2.5	µA
Maximum Quiescent Supply Current	I_{CC}	5.5V	V_{IN} = V_{CC} or GND, I_{OUT} = 0µA	4	40	40	µA

5. -40˚C ≤ T_J ≤ +85˚C

AC Electrical Characteristics[6] (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum Clock Frequency (Figure 5)	f_{min}	3.3V ±0.3V	C_L = 15pF	80	60	60	MHz
			C_L = 50pF	55	40	40	
		5V ±0.5V	C_L = 15pF	135	110	110	
			C_L = 50pF	95	85	85	

6. Not production tested in die form, characterized by chip design and tested in package.

AC Electrical Characteristics[6] Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Maximum Propagation delay from input RCLK to output Q_A-Q_H (Figure 3,5)	t_{PLH}, t_{PHL}	3.3V ±0.3V	C_L = 15pF	13	14	14	ns
			C_L = 50pF	16	17.2	17.2	
		5V ±0.5V	C_L = 15pF	9	10	10	
			C_L = 50pF	11	12	12	
Maximum Propagation delay from input SRCLK to output QH' (Figure 3, 5)	t_{PLH}, t_{PHL}	3.3V ±0.3V	C_L = 15pF	13	15	15	ns
			C_L = 50pF	16.5	18.5	18.5	
		5V ±0.5V	C_L = 15pF	8.2	9.4	9.4	
			C_L = 50pF	11	11.4	11.4	
Maximum Propagation delay from input $\overline{SRCLR}$ to output QH' (Figure 3, 5)	t_{PHL}	3.3V ±0.3V	C_L = 15pF	12.8	13.7	13.7	ns
			C_L = 50pF	16.3	17.2	17.2	
		5V ±0.5V	C_L = 15pF	8	9.1	9.1	
			C_L = 50pF	10	11.1	11.1	
Maximum Propagation delay from input $\overline{OE}$ to output Q_A-Q_H (Figure 4, 5)	t_{PZH}, t_{PZL}	3.3V ±0.3V	C_L = 15pF	11.5	13.5	13.5	ns
			C_L = 50pF	15	17	17	
		5V ±0.5V	C_L = 15pF	8.6	10	10	
			C_L = 50pF	10.6	12	12	
	t_{PHZ}, t_{PLZ}	3.3V ±0.3V	C_L = 15pF	15.7	16.2	16.2	ns
			C_L = 50pF	10.3	11	11	
		5V ±0.5V	C_L = 15pF	15.7	16.2	16.2	
			C_L = 50pF	10.3	11	11	

Timing Requirements (Voltages referenced to GND)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			25°C	85°C	FULL RANGE[5]	
Minimum pulse duration, SRCLK high or low (Figure 1,5)	t_w	3.3V ±0.3V	5	5	5	ns
		5V ±0.5V	5	5	5	
Minimum pulse duration, RCLK high or low (Figure 1, 5)		3.3V ±0.3V	5	5	5	
		5V ±0.5V	5	5	5	
Minimum pulse duration, $\overline{SRCLR}$ low (Figure 1,5)		3.3V ±0.3V	5	5	5	
		5V ±0.5V	5	5	5	

Timing Requirements Continued

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			25°C	85°C	FULL RANGE[5]	
Minimum setup time, SER before SRCLK↑ (Figure 2,5)	t_{SU}	3.3V ±0.3V	3.5	3.5	3.5	ns
		5V ±0.5V	3	3	3	
Minimum setup time, SRCLK↑ before RCLK↑ (Figure 2,5)		3.3V ±0.3V	8	8	8	
		5V ±0.5V	5	5	5	
Minimum setup time, $\overline{\text{SRCLR}}$ low before RCLK↑ (Figure 2,5)		3.3V ±0.3V	8	8	8	
		5V ±0.5V	5	5	5	
Minimum setup time, $\overline{\text{SRCLR}}$ high(inactive) before SRCLK↑		3.3V ±0.3V	3	3	3	
		5V ±0.5V	2.5	2.5	2.5	
Minimum hold time, SER after SRCLK↑ (Figure 2,5)	t_H	3.3V ±0.3V	1.5	1.5	1.5	ns
		5V ±0.5V	2	2	2	

Operating Characteristics (V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Capacitance	C_{IN}	V_{IN} = V_{CC} or GND	-	3	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = V_{CC} or GND	-	5.5	-	
Power Dissipation Capacitance[7]	C_{PD}	No load, f = 1MHz	-	25.2	-	

7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

Switching Waveforms

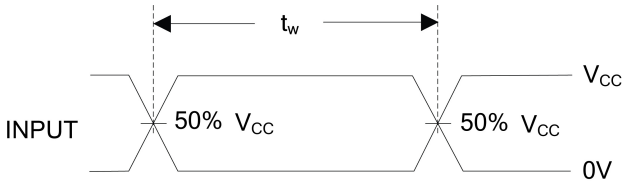


Figure 1 – Pulse duration

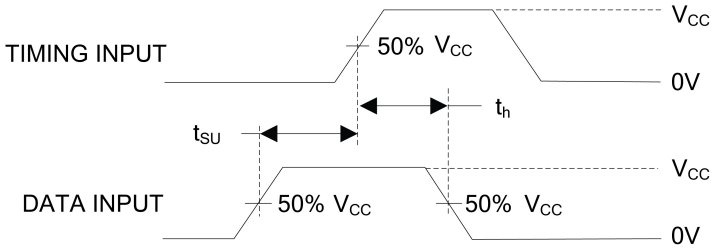


Figure 2 – Data setup and hold timing

Switching Waveforms continued

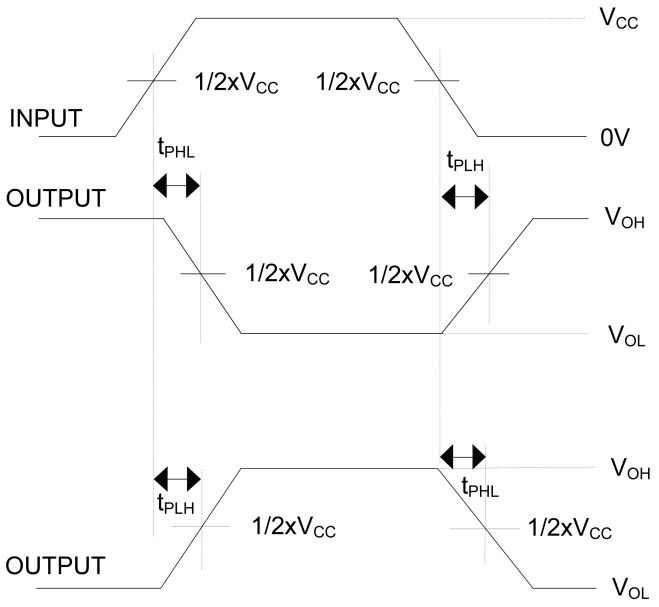


Figure 3 – Propagation delay timing

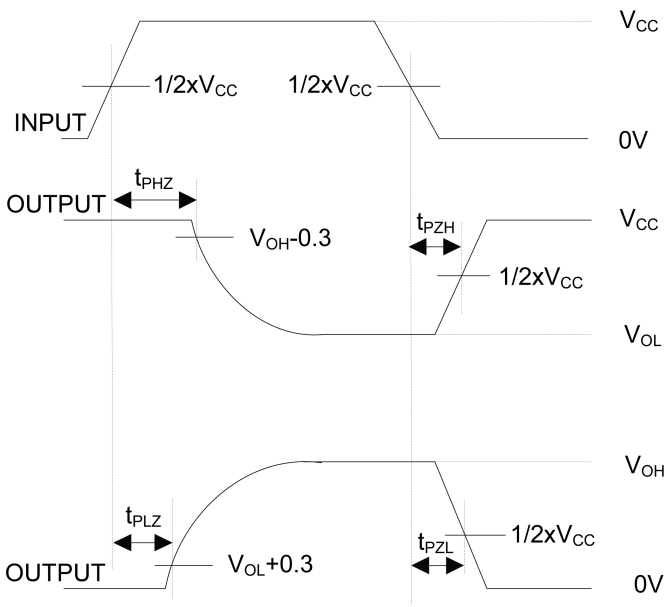
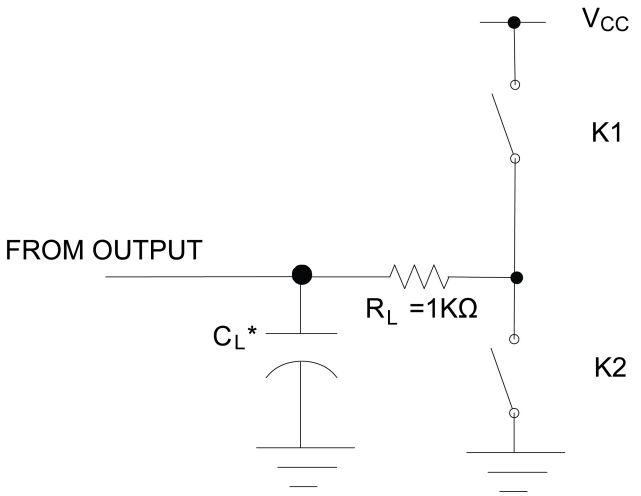


Figure 4 – 3-State enable & disable timing for $\overline{OE}$.



* Includes all probe and jig capacitance

TEST	K1	K2
t_{PLH}, t_{PHL}	OPEN	OPEN
t_{PHZ}, t_{PZH}	OPEN	CLOSE
t_{PLZ}, t_{PZL}	CLOSE	OPEN

Figure 5 – Load Circuit & Test Setup [8, 9]

8. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O=50Ω, t_r ≤3ns, t_f ≤3ns.
9. Outputs measured one at a time with one input transition per measurement.

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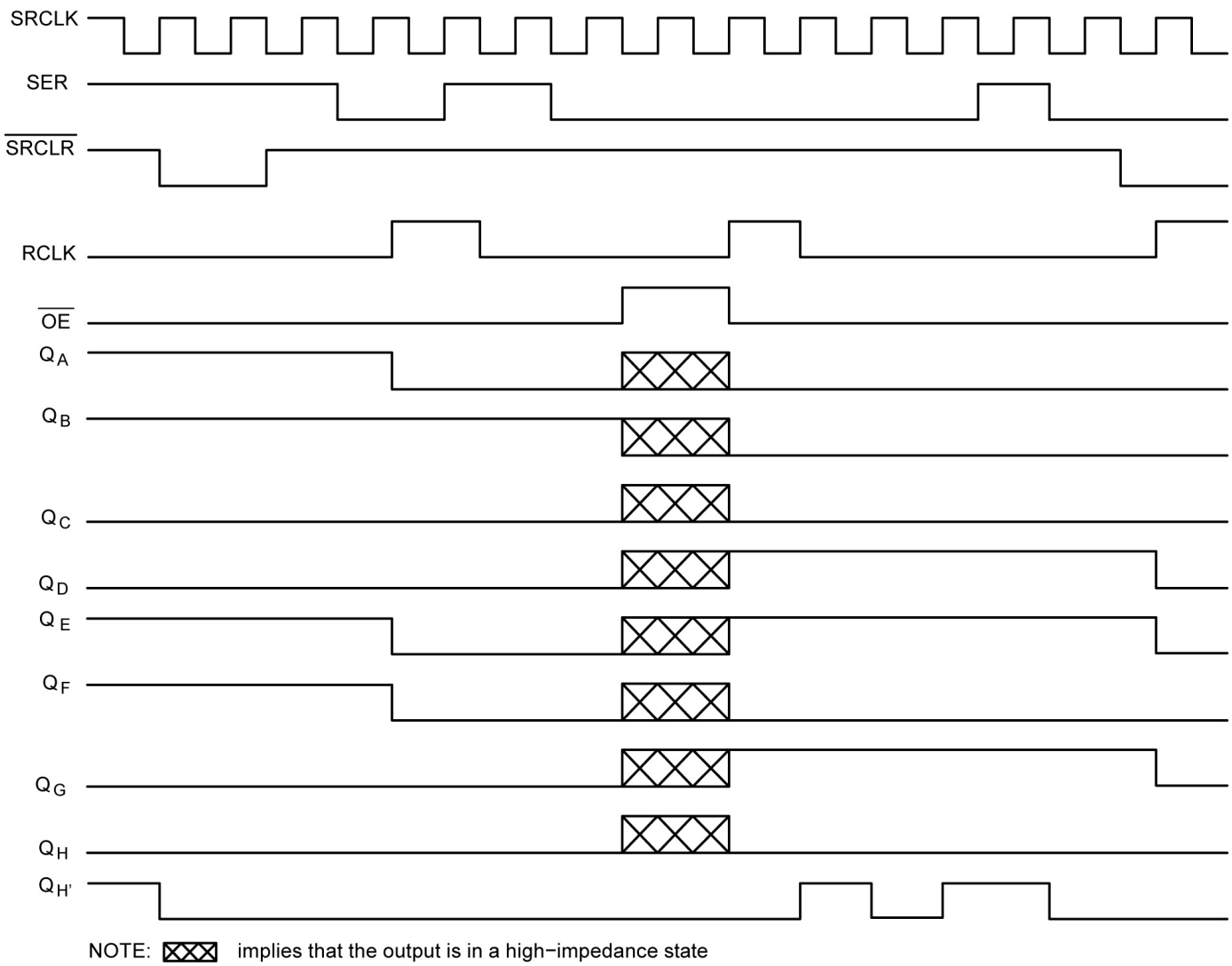
Timing Diagram



NOTE: ⊠ implies that the output is in a high−impedance state