

Quadruple 2-Input Exclusive OR Gate IC in bare die form

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Description

The 74ACT86 exclusive OR gate (XOR) is fabricated using a 1.5µm advanced CMOS process which combines the high speed performance of LSTTL with CMOS low power consumption. This device contains four independent gates and performs the Boolean functions Y = A \oplus B or Y = \overline{AB} + \overline{AB} . Device inputs directly accept LSTTL or CMOS. All inputs are protected against ESD and excess voltage transients.

Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 74LS86
- Lower power alternative to bipolar logic.

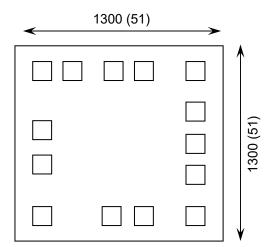
Ordering Information

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see 54ACT86

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

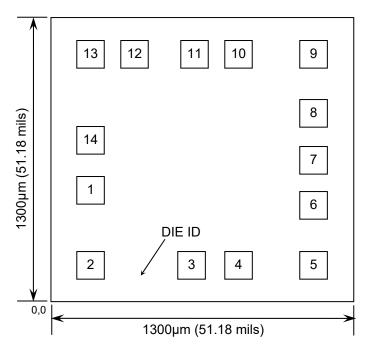
Die Size (Unsawn)	1300 x 1300 51 x 51`	µm mils	
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils	
Top Metal Composition	Al 1%Si 1.1μ	m	
Back Metal Composition	N/A – Bare Si		





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Pad Layout and Functions



PAD	FUNCTION	COORDIN	ATES (µm)					
FAD	TONCTION	X	Y					
1	A1 100		439					
2	B1	100	100					
3	Y1	547	100					
4	A2	751	100					
5	B2	1088	100					
6	Y2	1088	372					
7	GND	1088	579					
8	Y3	1088	797					
9	A3	1088	1070					
10	В3	751	1070					
11	Y4	566	1070					
12	A4	290	1070					
13	B4	100	1070					
14	V _{CC}	100	671					
CON	CONNECT CHIP BACK TO V _{CC} OR FLOAT							

Logic Diagram

A1
$$\frac{1}{2}$$
 3 Y1

A2 $\frac{4}{5}$ 6 Y2

 $Y = A \oplus B$
 $= \overline{A}B + A\overline{B}$

A3 $\frac{9}{10}$ 8 Y3

A4 $\frac{12}{13}$ 11 Y4

Function Table

INPUTS		OUTPUT				
Α	В	Υ				
L	L	L				
L	H H	H				
Н	L	Н				
Н	Н	L				
H = High level (steady state)						
$L = L_0$	ow leve	el (steady state)				





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-0.5 to V _{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
DC Input Current	I _{IN}	±20	mA
DC Output Current, per pad	I _{OUT}	±50	mA
DC Supply Current, V _{CC} or GND, per pad	I _{CC}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages Referenced to GND)

			`		
PARAMETER	2	SYMBOL	MIN	MAX	UNITS
DC Supply Voltage	V _{CC}	4.5	5.5	V	
DC Input or Output Voltage		V_{IN} , V_{OUT}	0	V _{CC}	V
Operating Temperature Ran	T _J	-40	+85	°C	
Output current - High		I _{OH}	-	-24	mA
Output current - Low		I _{OL}	-	24	mA
Input Rise or Fall rate V _{CC} = 4.5		Δt/ΔV	0	10	ns/V
(V _{IN} from 0.8V to 2V)	$V_{CC} = 5.5V$		0	8	115/ V

^{3.} This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND \leq (V_{IN} or V_{OUT}) \leq V_{CC} . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIMI	ΓS	UNITS
	OTHEOL	• 66	GONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS
Minimum High-Level	V _{IH}	4.5V	$V_{OUT} = 0.1V$	2	2	2	V
Input Voltage	VIH	5.5V	or V _{CC} -0.1V	2	2	2	V
Maximum Low-Level	V _{IL}	4.5V	001	0.8	0.8	0.8	V
Input Voltage		5.5V	or V _{CC} -0.1V	0.8	0.8	0.8	V
		4.5V	/ Ι _{ΟυΤ} = 50μΑ	0.1	0.1	0.1	V
		5.5V	1001 – 30μΑ	0.1	0.1	0.1	V
Minimum Low-Level	V _{OL}	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	0.36	0.44	0.44	V
Output Voltage	V OL	5.5V	$I_{OL} = 24mA$	0.36	0.44	0.44	V
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^{5,6}$	-	-	1.65	V
		5.5V	$I_{OL} = 75 \text{mA}$	-	-	1.65	V

^{4. -55°}C ≤ T_J ≤ +125°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75 Ω transmission-line drive capability at 125°C





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DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	DITIONS		ΓS	UNITS
TANAMETER	OTHIDOL	▼CC	CONDITIONS	25°C	85°C	FULL RANGE⁴	Oitilo
		4.5V	I _{OUT} = 50μA	4.4	4.4	4.4	V
Minimum High-Level	V _{OH}	5.5V	1001 – 30μΑ	5.4	5.4	5.4	V
Output Voltage	V OH	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	3.86	3.76	3.76	V
		5.5V	$I_{OH} = -24mA$	4.86	4.76	4.76	V
Maximum Input Leakage Current	I _{IN}	5.5V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	μA
Additional Maximum I _{CC} / Input	ΔI _{CCT}	5.5V	V _{IN} = V _{CC} -2.1V	0.6	1.5	1.5	mA
Minimum Dynamic	I _{OLD}	5.5V	V _{OLD} = 1.65V Max	-	75	75	mA
Output Current ⁷	I _{OHD}	5.5V	V _{OHD} = 3.85V Min	-	-75	-75	ША
Maximum Quiescent Supply Leakage Current	I _{CC}	5.5V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	40	μА

^{7.} Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics⁸ V_{CC} = 5.0V ±0.5V

PARAMETER SY	SYMBOL	V _{cc}	CONDITIONS	CONDITIONS LIMITS 25°C 85°C FULL RANGE ⁴	UNITS		
	OTHEOL	▼ CC	CONDITIONS		85°C	FULL RANGE⁴	Oitiio
Maximum Propagation Delay	t _{PLH}	5.0V	C _L = 50pF,	9.5	10	10	
Input A or B to Output Y (Figure 1)	t _{PHL}	5.0V	Input $tr = tf = 3.0$ ns	9.5	10.5	10.5	ns
Maximum Input	C _{IN}	5.0V	T _J = 25°C		TYPIC	AL	pF
Capacitance	OIN	0.01	15 20 0		4.5		Pi
Power Dissipation Capacitance	C _{PD}	5.0V	$T_J = 25$ °C, $C_L = 50$ pF		35		pF

^{8.} Not production tested in die form, characterized by chip design.





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Switching Waveform

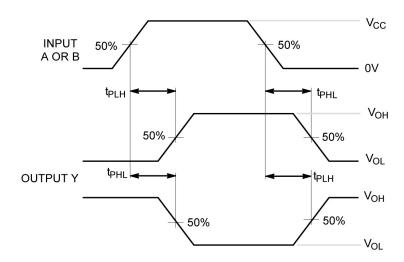


Figure 1 - Propagation Delay

Test Circuit $1k\Omega \nearrow R_{pd}$ OUTPUT C_{L}^{*} C_{L}^{*}

* Includes all probe and jig capacitance

Figure 2

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