



Advanced CMOS TTL Input – 74ACT74

Dual D-Type Flip-Flop Logic IC with Set and Reset in bare die form

Rev 1.0
21/11/19

Description

The 74ACT74 is fabricated using a 1.5µm advanced 5V CMOS process & consists of two identical, independent data type flip-flops. Each flip-flop has separate data, set, reset, clock inputs & Q, Q̄ outputs. The device can be used in Shift Register applications and also Counter or Toggle applications by connecting Q output to the data input. The logic level present at the “D” input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is clock independent and accomplished by a high level on the respective Set or Reset line.

Features:

- Inputs directly accept TTL
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Outputs Source/Sink 24 mA
- Asynchronous Set-Reset Capability
- Lower power alternative to bipolar logic
- Functionally compatible with bipolar 74LS74
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

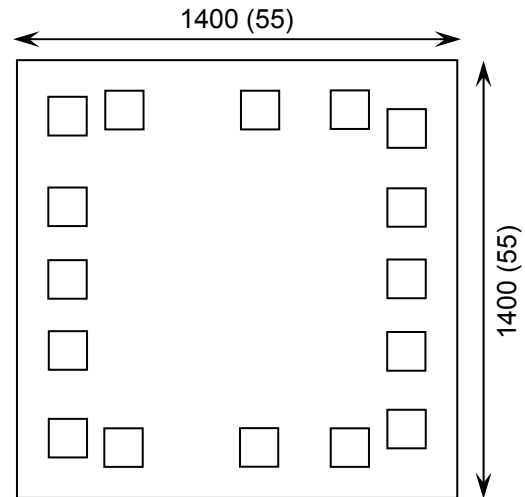
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54ACT74](#)

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1400 x 1400 55 x 55	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

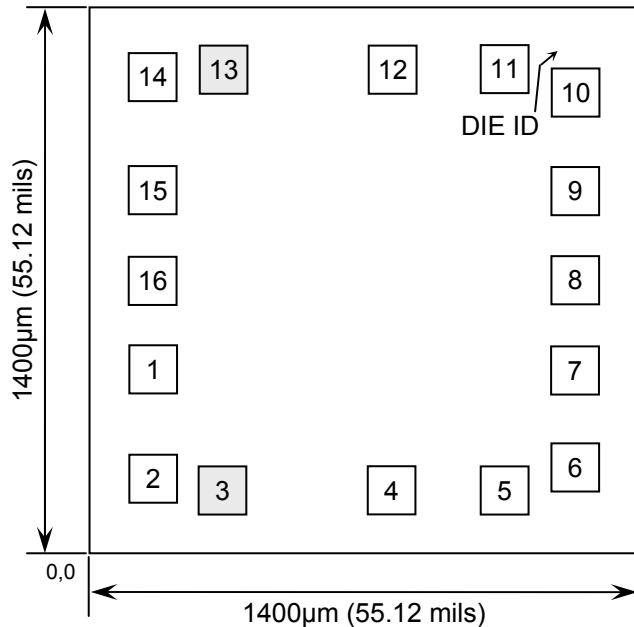




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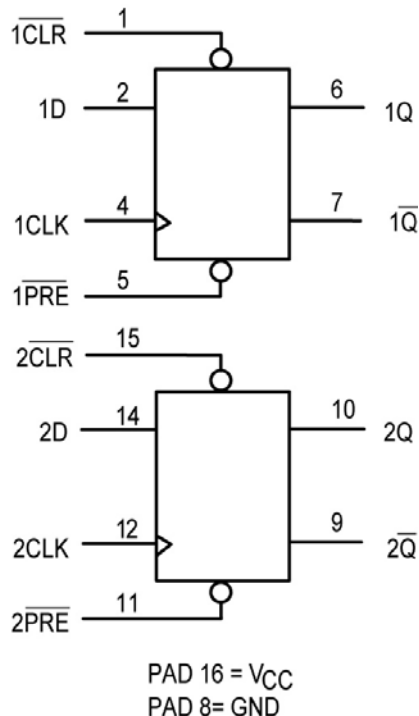
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1 $\overline{\text{CLR}}$	0.100	0.410
2	1D	0.100	0.130
3	NO CONNECT	0.280	0.100
4	1CLK	0.710	0.100
5	1 $\overline{\text{PRE}}$	1.00	0.100
6	1Q	1.180	0.160
7	1 $\overline{\text{Q}}$	1.180	0.410
8	GND	1.180	0.640
9	2 $\overline{\text{Q}}$	1.180	0.870
10	2Q	1.180	1.120
11	2 $\overline{\text{PRE}}$	1.00	1.180
12	2CLK	0.710	1.180
13	NO CONNECT	0.280	1.180
14	2D	0.100	1.160
15	2 $\overline{\text{CLR}}$	0.100	0.870
16	V _{CC}	0.100	0.640

CONNECT CHIP BACK TO V_{CC} OR FLOAT

Logic Diagram



Truth Table

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↘	L	L	H
H	H	L	X	No Change	No Change
H	H	H	X	No Change	No Change
H	H	↔	X	No Change	No Change

* BOTH OUTPUTS WILL REMAIN HIGH AS LONG AS SET AND RESET ARE LOW, OUTPUT STATES ARE UNPREDICTABLE IF SET AND RESET GO HIGH SIMULTANEOUSLY.





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input or Output Voltage (Referenced to GND)	V_{IN}, V_{OUT}	-0.5 to $V_{CC}+0.5$	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±20	mA
Output Current (per Pad)	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air ²	P_D	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages Referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	V_{CC}	4.5	5.5	V	
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	V_{CC}	V	
Operating Temperature Range	T_J	-40	+85	°C	
Output current - High	I_{OH}	-	-24	mA	
Output current - Low	I_{OL}	-	24	mA	
Input Rise or Fall rate (V_{IN} from 0.8V to 2V)	$\Delta t/\Delta V$	$V_{CC} = 4.5V$	0	10	ns/V
		$V_{CC} = 5.5V$	0	8	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum High-Level Input Voltage	V_{IH}	4.5V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum Low-Level Output Voltage	V_{OL}	4.5V	$I_{OUT} = 50\mu A$	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$ $I_{OL} = 24mA$	0.36	0.44	0.44	V
		5.5V		0.36	0.44	0.44	
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^{5,6}$ $I_{OL} = 75mA$	-	-	1.65	V
		5.5V		-	-	1.65	

4. $-40^\circ C \leq T_J \leq +85^\circ C$ 5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C





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DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum High-Level Output Voltage	V _{OH}	4.5V	I _{OUT} = -50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OL} = -24mA	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	
		4.5V	V _{IN} = V _{IL} or V _{IH} ^{5,6} I _{OL} = -75mA	-	-	3.85	V
		5.5V		-	-	3.85	
Maximum Input Leakage Current	I _{IN}	5.5V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	µA
Additional Maximum I _{CC} / Input	ΔI _{CCT}	5.5V	V _{IN} = V _{CC} -2.1V	0.6	1.5	1.5	mA
Minimum Dynamic Output Current ⁷	I _{OLD}	5.5V	V _{OLD} = 1.65V Max	-	75	75	mA
	I _{OHD}	5.5V	V _{OHD} = 3.85V Min	-	-75	-75	
Maximum Quiescent Supply Leakage Current	I _{CC}	5.5V	V _{IN} = V _{CC} or GND I _{OUT} = 0µA	4	40	40	µA

7. Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics⁸

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Clock Frequency	f _{max}	5V ±10%	-	145	125	125	MHz
Maximum Propagation Delay, CLK to Q or Q (Figure1)	t _{PLH}	5V ±10%	C _L = 50pF, Input t _r = t _f = 3ns	11	13	13	ns
	t _{PHL}			10	11.5	11.5	
Maximum Propagation Delay, PRE or CLR to Q or Q (Figure 2)	t _{PLH}	5V ±10%	C _L = 50pF, Input t _r = t _f = 3ns	9.5	10.5	10.5	ns
	t _{PHL}			10	11.5	11.5	
Maximum Input Capacitance	C _{IN}	5V ±10%	V _{IN} = V _{CC} or GND	4.5	4.5	4.5	pF
Power Dissipation Capacitance ⁹	C _{PD}	-	T _J = 25°C, V _{CC} = 5.0V	TYPICAL			pF
				35			

8. Not production tested in die form, characterized by chip design and tested in package.

9. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.





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Timing Requirements⁸

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum Setup Time, D to CLK (Figure 3)	t _{SU}	5V ±10%	C _L = 50pF, Input t _r = t _f = 3ns	3	3.5	3.5	ns
Minimum Hold Time, CLK to D (Figure 3)	t _H	5V ±10%	C _L = 50pF, Input t _r = t _f = 3ns	1	1	1	ns
Minimum Pulse Width, CLK, $\overline{\text{PRE}}$, $\overline{\text{CLR}}$ (Figure 1)	t _w	5V ±10%	C _L = 50pF, Input t _r = t _f = 3ns	5	6	6	ns
Maximum Recovery Time, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK (Figure 2)	t _{rec}	5V ±10%	C _L = 50pF, Input t _r = t _f = 3ns	0	0	0	ns

Switching Waveforms

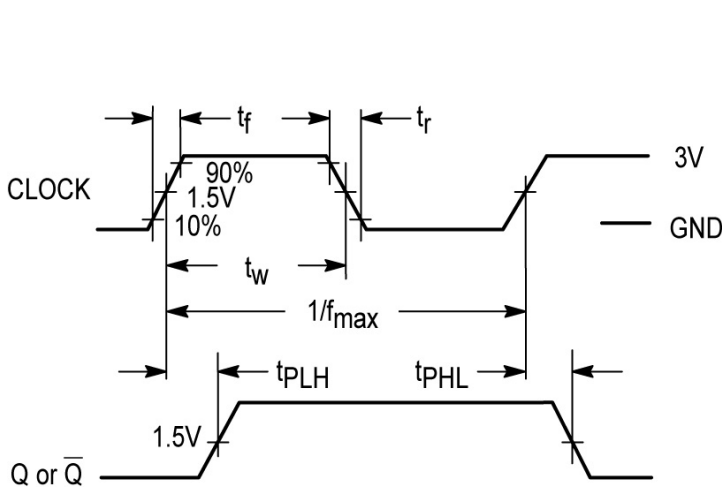


Figure 1 – Data, Clock and Output

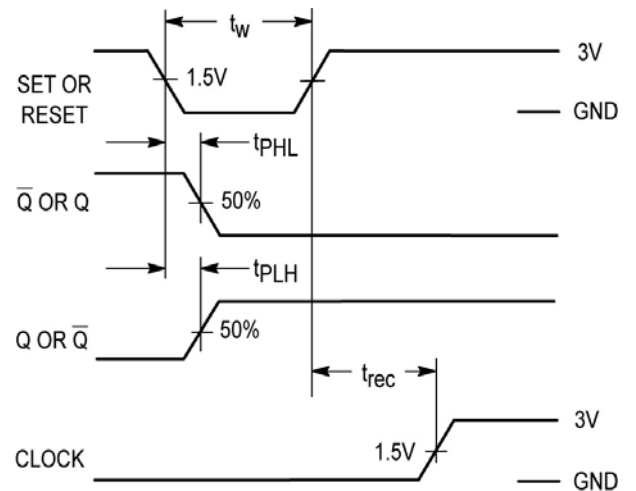


Figure 2 – Set, Reset, Clock and Output





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Switching Waveforms continued

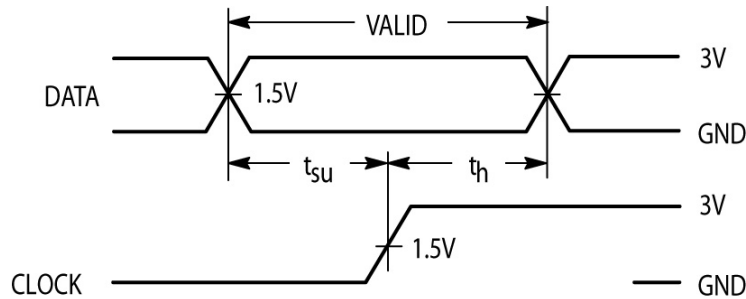
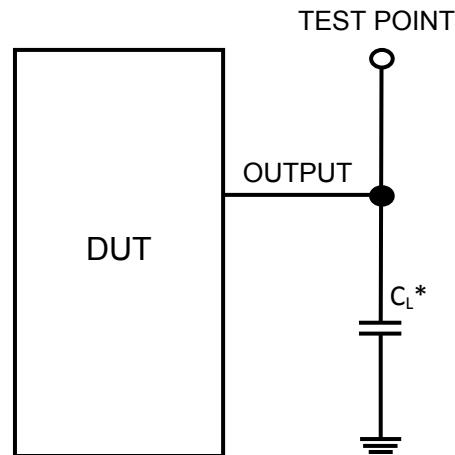


Figure 3 – Clock to Data

Test Circuit



* Includes all probe and jig capacitance

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