



# Advanced CMOS TTL Input – 74ACT244

Octal 3-State Non-Inverting Buffer / Line Driver / Line Receiver in bare die form

Rev 1.0  
24/04/19

## Description

The 74ACT244 is produced on a 1.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device can be used as two 4-bit buffers or one 8-bit buffer & features non-inverting inputs with two output enables, each controlling four of the 3-state outputs. The device is designed to improve performance & density in clock drivers, 3-state memory address drivers & bus orientated transmitters and receivers. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ . Device inputs directly accept TTL without use of pull-up resistors.

## Features:

- Outputs Source/Sink 24mA
- Low input current: 1µA
- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Operating voltage range: 4.5V to 5.5V
- Function compatible with 74LS244
- Lower power alternative to bipolar logic.

## Ordering Information

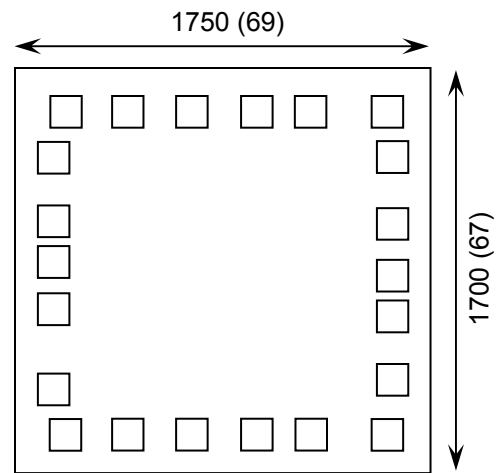
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54ACT244](#)

## Die Dimensions in µm (mils)



## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1750 x 1700 69 x 67	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

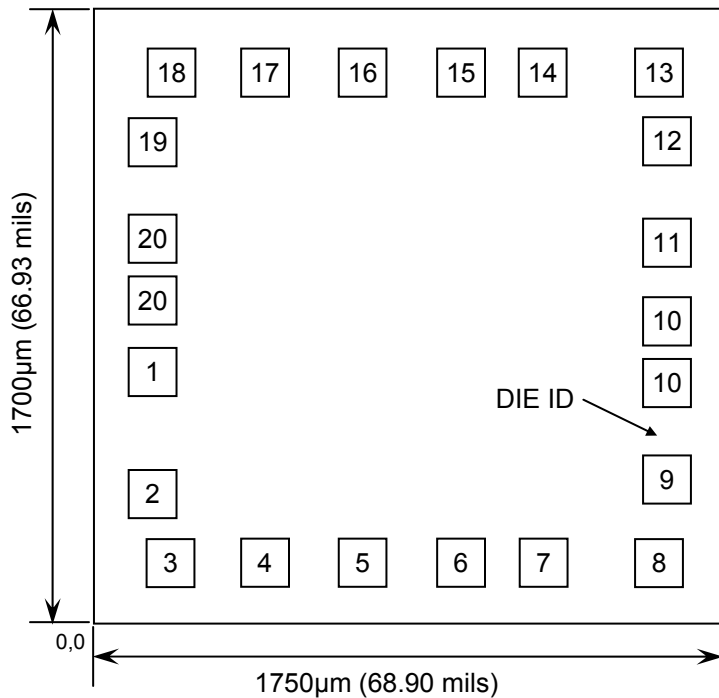




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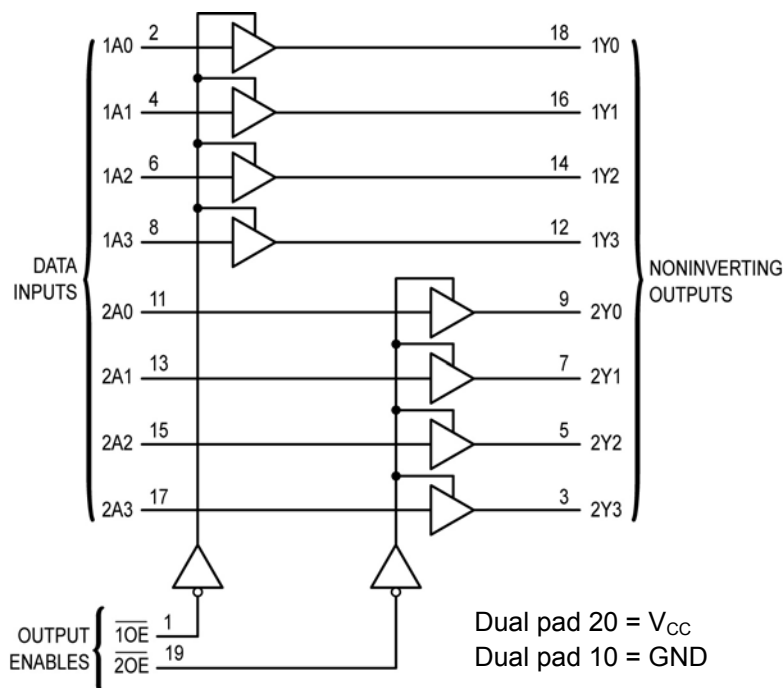
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1OE}$	0.100	0.630
2	1A0	0.100	0.290
3	2Y3	0.150	0.100
4	1A1	0.410	0.100
5	2Y2	0.680	0.100
6	1A2	0.950	0.100
7	2Y1	1.180	0.100
8	1A3	1.500	0.100
9	2Y0	1.520	0.330
10	GND	1.520	0.600
10	GND	1.520	0.770
11	2A0	1.520	0.990
12	1Y3	1.520	1.270
13	2A1	1.500	1.460
14	1Y2	1.180	1.460
15	2A2	0.950	1.460
16	1Y1	0.680	1.460
18	1Y0	0.150	1.460
19	$\overline{2OE}$	0.100	1.270
20	V <sub>CC</sub>	0.100	1.000
20	V <sub>CC</sub>	0.100	0.830

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

## Logic Diagram



## Truth Table

INPUTS		OUTPUTS
$\overline{1OE}$ $\overline{2OE}$	1A, 2A	1Y, 2Y
L	L	L
L	H	H
H	X	Z

H = High level (steady state)  
L = Low level (steady state)  
X = Don't care, Z = High impedance





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## Pad Descriptions

### ADDRESS INPUTS

1A0, 1A1, 1A2, 1A3, 2A0, 2A1, 2A2, 2A3

(Pads 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROL INPUTS

1OE, 2OE (Pads 1, 19)

Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as non-inverting buffers. When a high level is applied, the outputs assume the high impedance state.

### OUTPUTS

1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3

(Pads 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output– enable pins, these outputs are either non-inverting outputs or high–impedance outputs.

## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current, per pin	$I_{IN}$	±20	mA
DC Output Current, per pin	$I_{OUT}$	±50	mA
DC $V_{CC}$ or GND Current, per pin	$I_{CC}$	±50	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	$V_{CC}$	4.5	5.5	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	0	+85	°C	
Output current - High	$I_{OH}$	-	-24	mA	
Output current - Low	$I_{OL}$	-	24	mA	
Input Rise or Fall rate ( $V_{IN}$ from 0.8V to 2V)	$\Delta t/\Delta V$	$V_{CC} = 4.5V$	0	10	ns/V
		$V_{CC} = 5.5V$	0	8	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.





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## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	V <sub>IH</sub>	4.5V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V <sub>IL</sub>	4.5V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V <sub>OH</sub>	4.5V	I <sub>OUT</sub> = -50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> <sup>4</sup> I <sub>OH</sub> = -24mA	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	4.5V	I <sub>OUT</sub> = 50µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> <sup>4</sup> I <sub>OL</sub> = 24mA	0.36	0.44	0.44	V
		5.5V		0.36	0.44	0.44	
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State leakage current	I <sub>OZ</sub>	5.5V	V <sub>OUT</sub> = V <sub>CC</sub> or GND V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	±0.5	±2.5	±2.5	µA
Additional Maximum I <sub>CC</sub> / Input	ΔI <sub>CCT</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> - 2.1V	1	1.5	1.5	mA
Minimum Dynamic Output Current <sup>6</sup>	I <sub>OLD</sub>	5.5V	V <sub>OLD</sub> = 1.65V Max	-	75	75	mA
	I <sub>OHD</sub>	5.5V	V <sub>OHD</sub> = 3.85V Min	-	-75	-75	
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0µA	8	40	40	µA

4. 0°C ≤ T<sub>J</sub> ≤ +85°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics<sup>7</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Propagation Delay 1A to 1Y or 2A to 2Y	t <sub>PLH</sub> , t <sub>PHL</sub>	5V ±0.5	C <sub>L</sub> = 50pF	9	10	10	ns
Output Enable Time OE to 1Y or 2Y	t <sub>PZH</sub>	5V ±0.5	C <sub>L</sub> = 50pF	8.5	9.5	9.5	ns
	t <sub>PZL</sub>			9.5	10.5	10.5	
Output Disable Time OE to 1Y or 2Y	t <sub>PHZ</sub>	5V ±0.5	C <sub>L</sub> = 50pF	9.5	10.5	10.5	ns
	t <sub>PLZ</sub>			10	10.5	10.5	

7. Not production tested in die form, characterized by chip design and tested in package.





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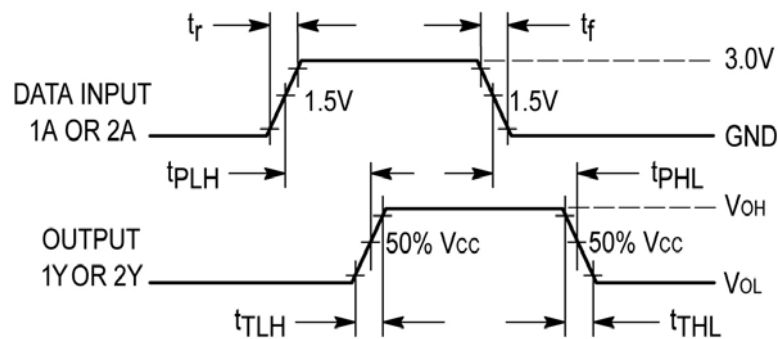
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## Capacitance<sup>7</sup>

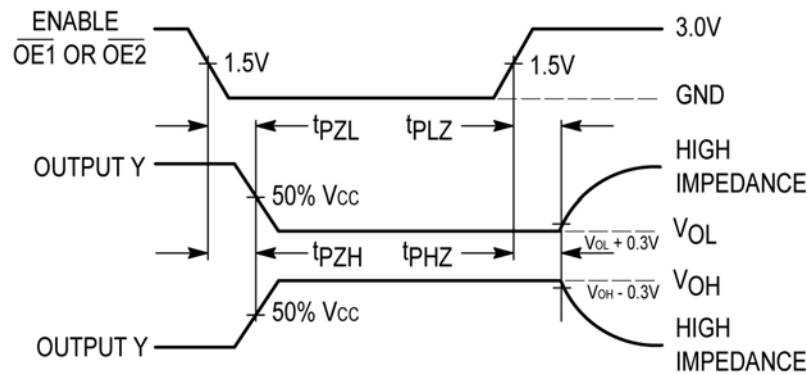
PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	TYPICAL	UNITS
Maximum Input Capacitance	C <sub>IN</sub>	5.0V	T <sub>A</sub> = 25°C	4.5	pF
Power Dissipation Capacitance (Per Buffer/Driver)	C <sub>PD</sub>	5.0V	T <sub>A</sub> = 25°C, C <sub>L</sub> = 50pF, F = 1MHz	45	pF

7. Not production tested in die form, characterized by chip design and tested in package.

## Switching Waveforms



**Figure 1** – Propagation Delay - Input 1A or 2A to Output 1Y or 2Y



**Figure 2** – Propagation Delay - Output Enable to Output 1Y or 2Y

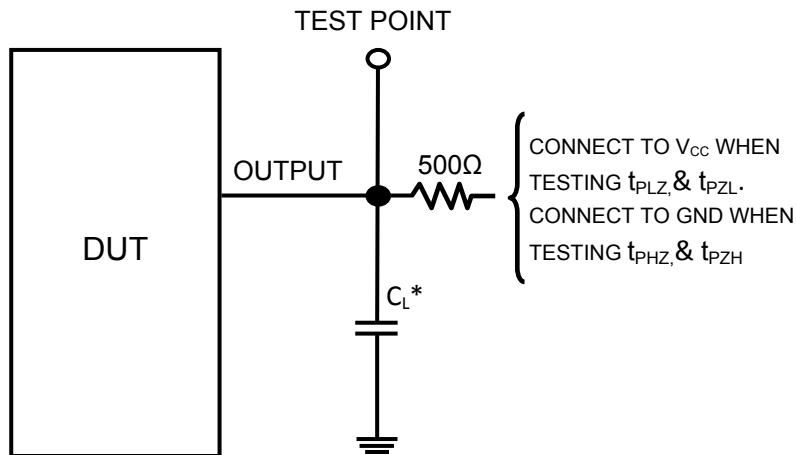




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## Test Circuit



\* Includes all probe and jig capacitance

Figure 3

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