Advanced CMOS TTL Input – 74ACT14

Hex Schmitt-Trigger Inverter with LSTTL compatible inputs in bare die form

Rev 1.0
11/03/19

Description

The 74ACT14 Hex Schmitt-Trigger Inverter is fabricated using an advanced CMOS process combining LSTTL speed with CMOS low power consumption while delivering high output drive. The device performs the Boolean function Y = Ā in positive logic. Device inputs directly accept LSTTL or CMOS. Schmitt-Trigger inputs transform slow input rise and fall times into sharply defined jitter-free output signals. Due to the hysteresis voltage of the Schmitt trigger, the 74ACT14 is useful in noisy environments. All inputs are protected against ESD and excess voltage transients.

Features:

- Schmitt Trigger Inputs
- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Sink/Source 24mA
- Low power dissipation: I_{CC} 2µA max at 25°C
- High noise immunity
- Functionally compatible with bipolar 74F14.

Ordering Information

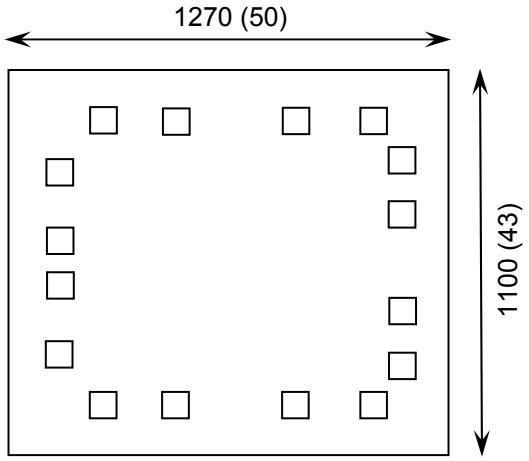
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT14

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1270 x 1100 50 x 43	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±20) 11.02 (±0.79)	µm mils
Top Metal Composition	Al-Si-Cu	
Back Metal Composition	N/A – Bare Si	

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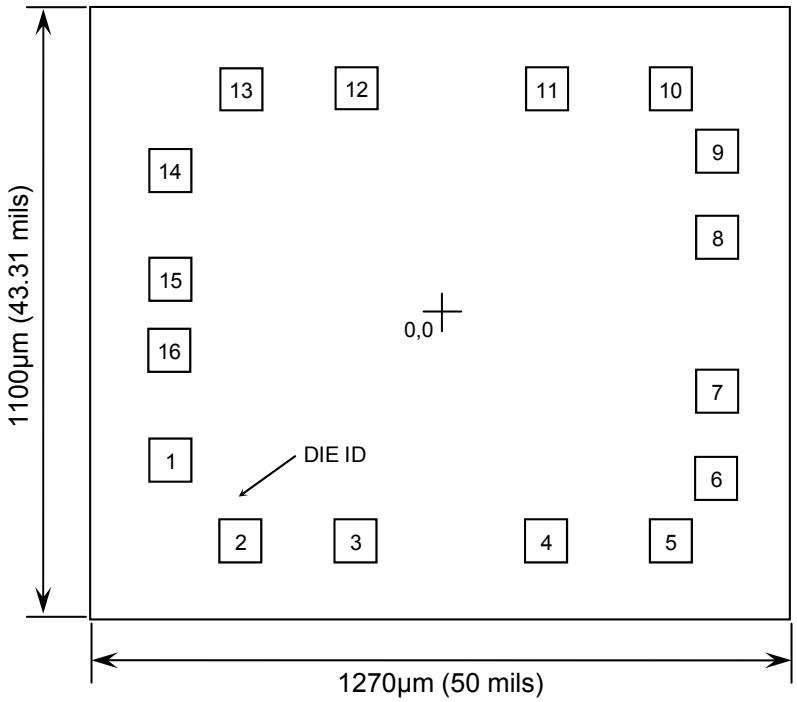
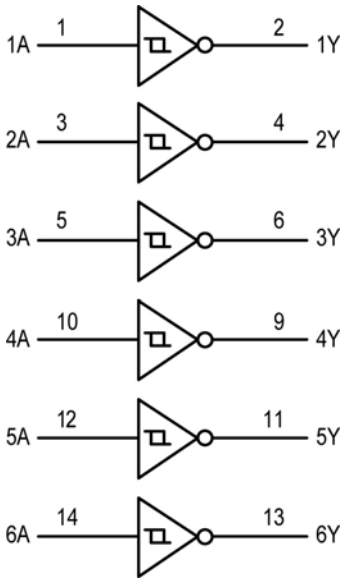
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1A	-502	-263.5
2	1Y	-364.9	-410
3	2A	-157.7	-410
4	2Y	188.9	-410
5	3A	413	-410
6	3Y	495	-298
7	GND	495	-140
8	GND	495	140
9	4Y	495	298
10	4A	413	410
11	5Y	188.9	410
12	5A	-157.7	410
13	6Y	-364.9	410
14	6A	-495	263
15	V_{CC}	-495	64.2
16	V_{CC}	-495	-64.2
CHIP BACK IS ISOLATED			

Logic Diagram



$Y = \bar{A}$

Pad 15,16 = V_{CC}
Pad 7,8 = GND

Function Table

INPUTS A	OUTPUT Y
H	L
L	H
H = High level (steady state)	
L = Low level (steady state)	

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions[2] (Voltages Referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_J	-40	+85	°C
Input Rise or Fall rate[3] (except Schmitt Inputs)	t_r, t_f	-	20	ns/V
Output Current – High	I_{OH}	-	-24	mA
Output Current – Low	I_{OL}	-	24	mA

2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. **3.** V_{IN} from 0.8V to 2.0V

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Positive-Going Input Threshold Voltage	$V_{T+ MAX}$	4.5V		2.0	2.0	2.0	V
		5.5V		2.1	2.1	2.1	
Minimum Positive-Going Input Threshold Voltage	$V_{T+ MIN}$	4.5V		1.2	1.2	1.2	V
		5.5V		1.4	1.4	1.4	
Maximum Negative-Going Input Threshold Voltage	$V_{T- MAX}$	4.5V		1.2	1.2	1.2	V
		5.5V		1.4	1.4	1.4	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Negative-Going Input Threshold Voltage	$V_{T- MIN}$	4.5V		0.6	0.6	0.6	V
		5.5V		0.8	0.8	0.8	
Maximum Hysteresis Voltage[5]	$V_{H MAX}$	4.5V		1.4	1.4	1.4	V
		5.5V		1.6	1.6	1.6	
Minimum Hysteresis Voltage[5]	$V_{H MIN}$	4.5V		0.4	0.4	0.4	V
		5.5V		0.5	0.5	0.5	
Minimum High-Level Output Voltage	V_{OH}	4.5V	$V_{IN} = V_{T+}$ $I_{OUT} = -50\mu A$	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	$V_{IN} = V_{T+}$ $I_{OUT} = -24mA$	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	
		5.5V	$V_{IN} = V_{T+}$ $I_{OH} = -50mA$[5]	3.85	3.85	3.85	V
Maximum Low-Level Output Voltage	V_{OL}	4.5V	$V_{IN} = V_{T-}$ $I_{OL} = 50\mu A$	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{T-}$ $I_{OL} = 24mA$	0.36	0.44	0.44	V
		5.5V		0.36	0.44	0.44	
		5.5V	$V_{IN} = V_{T-}$ $I_{OL} = 50Ma$[6]	1.65	1.65	1.65	V
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	2	20	20	µA
Maximum Additional I_{CC} / Input[7]	ΔI_{CC}	5.5V	One input at 3.4V, Other input at GND or V_{CC}	0.6	1.5	1.5	mA

5. $V_{H MIN} > (V_{T+ MIN}) - (V_{T- MAX})$; $V_{H MAX} = (V_{T+ MAX}) + (V_{T- MIN})$ **6.** Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms. **7.** This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0V or V_{CC}

AC Electrical Characteristics[8] (V_{CC} = 5.0V ±0.5V)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Input A to Output Y (Figure 1)	t_{PLH}	5.0V	C_L = 50pF	11.5	12.5	12.5	ns
	t_{PHL}	5.0V		10	11	11	

Capacitance[8] (V_{CC} = 5V, T_j = 25°C)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	TYPICAL	UNITS
Input Capacitance	C_{IN}	5V	$V_{IN} = V_{CC}$ or GND	4.5	pF
Power Dissipation Capacitance	C_{PD}	5V	C_L = 50pF, f = 1 MHz	45	pF

8. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

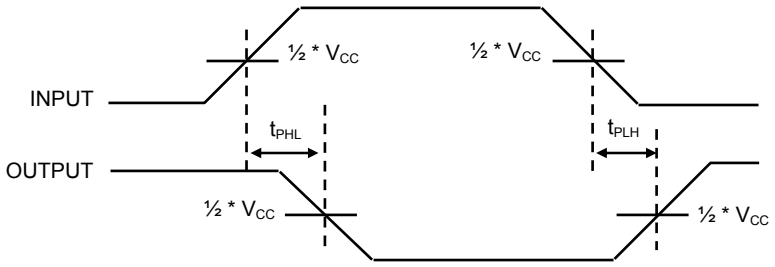

Figure 1 – Propagation Delay, Transition Timing

Test Circuit