Advanced CMOS TTL Input – 74ACT11

Triple 3-Input AND gate with LSTTL compatible inputs in bare die form

Rev 1.0
11/03/19

Description

The 74ACT11 is fabricated using an advanced CMOS process combining LSTTL speed with CMOS low power consumption while delivering high output drive. The device contains x3 independent gates each performing Boolean function $Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$ in positive logic. The device directly accepts LSTTL or NMOS inputs and suits use as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs. All inputs are protected against ESD and excess voltage transients.

Features:

- Inputs directly accept TTL / NMOS
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Sink/Source 24mA
- Low input current: 1µA
- High noise immunity
- Functionally compatible with bipolar 74LS/ALS11.
- Full military temperature Range

Ordering Information

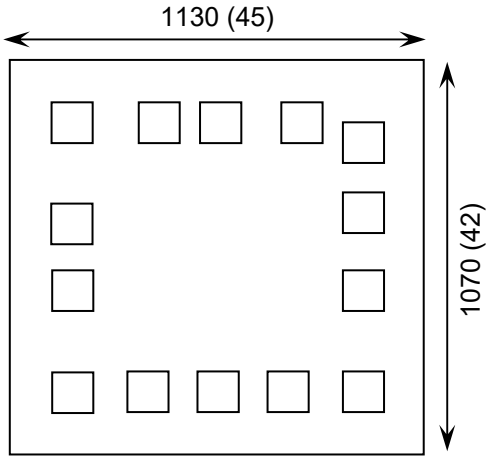
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT11

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1130 x 1070 45 x 42	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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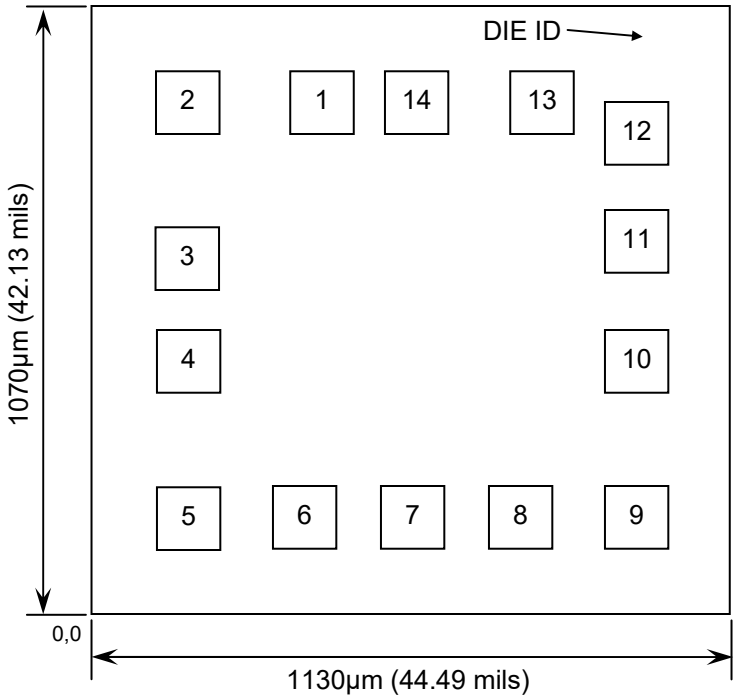
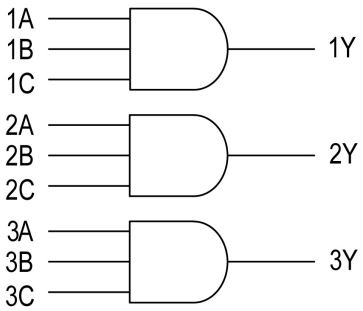
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1A	0.350	0.845
2	1B	0.115	0.845
3	2A	0.115	0.570
4	2B	0.115	0.390
5	2C	0.115	0.115
6	2Y	0.320	0.115
7	GND	0.510	0.115
8	3Y	0.705	0.115
9	3C	0.910	0.115
10	3B	0.910	0.390
11	3A	0.910	0.600
12	1Y	0.910	0.790
13	1C	0.740	0.845
14	V_{CC}	0.520	0.845
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Y = ABC

Truth Table

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

H = High level (steady state)
L = Low level (steady state)
X = Either Low or High level

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions[2] (Voltages Referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		4.5	5.5	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-40	+85	°C
Input Rise or Fall rate[3] (except Schmitt Inputs)	t_r, t_f	V_{CC} = 4.5V	0	10	ns/V
		V_{CC} = 5.5V	0	8	
Output Current – High	I_{OH}		-	-24	mA
Output Current – Low	I_{OL}		-	24	mA

2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. **3.** V_{IN} from 0.8V to 2.0V

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	I_{OUT} = -50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OH} = -24mA	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	I_{OUT} = 50µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = 24mA	0.36	0.44	0.44	V
		5.5V		0.36	0.44	0.44	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Additional Maximum I_{CC} / Input	ΔI_{CCT}	5.5V	V_{IN} = V_{CC} -2.1V	1	1.5	1.5	mA
Minimum Dynamic Output Current[6]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max	-	75	75	mA
	I_{OHD}	5.5V	V_{OHD} = 3.85V Min	-	-75	-75	
Maximum Quiescent Supply Leakage Current	I_{CC}	5.5V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	4	40	40	µA

5. All outputs loaded; thresholds on input associated with output under test. **6.** Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics[7]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Propagation Delay Input A,B,C to Output Y	t_{PLH}	5V ±0.5	C_L = 50pF, input t_r = t_f =3.0ns	9.5	10.5	10.5	ns
Propagation Delay Input A,B,C to Output Y	t_{PHL}	5V ±0.5	C_L = 50pF, input t_r = t_f =3.0ns	9.5	10.5	10.5	ns

Capacitance[7] (V_{CC} = 5V, T_j = 25°C)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS	UNITS
Input Capacitance	C_{IN}	5V	V_{IN} = V_{CC} or GND	4.5	pF
Power Dissipation Capacitance	C_{PD}	5V	C_L = 50pF, f = 1 MHz	TYPICAL	pF
				20	

7. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

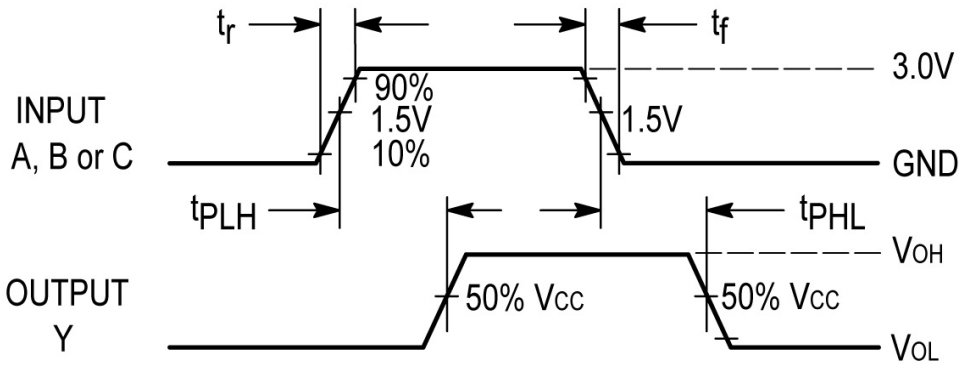
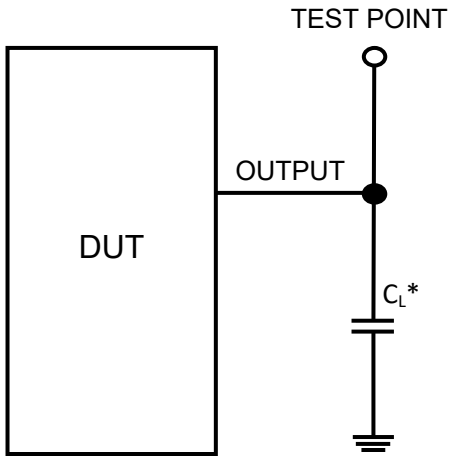


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



* Includes all probe and jig capacitance

Figure 2