

Triple 3-Input AND gate with LSTTL compatible inputs in bare die form

Rev 1.0 11/03/19

Description

The 74ACT11 is fabricated using an advanced CMOS process combining LSTTL speed with CMOS low power consumption while delivering high output drive. The device contains x3 independent gates each performing Boolean function Y = A • B • C or Y = \overline{A} + \overline{B} + \overline{C} in positive logic. The device directly accepts LSTTL or NMOS inputs and suits use as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs. All inputs are protected against ESD and excess voltage transients.

Ordering Information

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT11

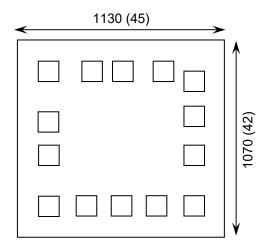
Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Features:

- Inputs directly accept TTL / NMOS
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Sink/Source 24mA
- Low input current: 1µA
- High noise immunity
- Functionally compatible with bipolar 74LS/ALS11.
- Full military temperature Range

Die Dimensions in µm (mils)



Mechanical Specification

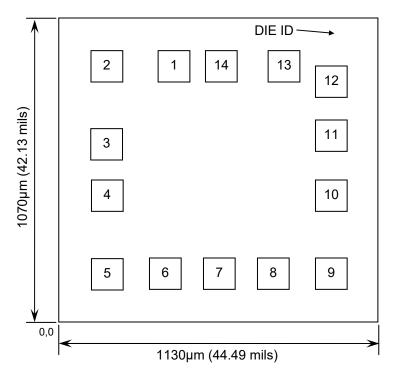
Die Size (Unsawn)	1130 x 1070 45 x 42	μm mils	
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	μm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils	
Top Metal Composition	Al 1%Si 1.1μ	m	
Back Metal Composition	N/A – Bare Si		





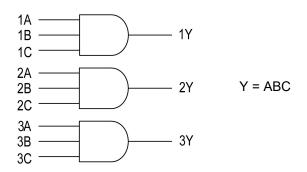
Rev 1.0 11/03/19

Pad Layout and Functions



D FUNCTION		ATES (µm)
	X	Υ
1A	0.350	0.845
1B	0.115	0.845
2A	0.115	0.570
2B	0.115	0.390
2C	0.115	0.115
2Y	0.320	0.115
GND	0.510	0.115
3Y	0.705	0.115
3C	0.910	0.115
3B	0.910	0.390
3A	0.910	0.600
1Y	0.910	0.790
1C	0.740	0.845
V _{CC}	0.520	0.845
	1B 2A 2B 2C 2Y GND 3Y 3C 3B 3A 1Y 1C V _{CC}	1B 0.115 2A 0.115 2B 0.115 2C 0.115 2Y 0.320 GND 0.510 3Y 0.705 3C 0.910 3B 0.910 3A 0.910 1Y 0.910 1C 0.740

Logic Diagram



Truth Table

II	NPUTS	OUTPUT	
Α	В	С	Y
H L X X	H X L X	H X X L	H L L

H = High level (steady state)

L = Low level (steady state)

X = Either Low or High level





Rev 1.0 13/05/21

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-0.5 to V _{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
DC Input Current	I _{IN}	±20	mA
DC Output Current, per pad	I _{OUT}	±50	mA
DC Supply Current, V _{CC} or GND, per pad	I _{cc}	±50	mA
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions² (Voltages Referenced to GND)

			\		- /
PARAMETER	S	YMBOL	MIN	MAX	UNITS
Supply Voltage		V _{CC}		5.5	V
DC Input or Output Voltage	V _{IN} ,V _{OUT}		0	V _{CC}	V
Operating Temperature Range	TJ		-40	+85	°C
Input Rise or Fall rate ³	+ +.	V _{CC} = 4.5V	0	10	ns/V
(except Schmitt Inputs)	t _r , t _f	V _{CC} = 5.5V	0	8	115/ V
Output Current – High		I _{OH}	-	-24	mA
Output Current – Low		I _{OL}	-	24	mA

^{2.} This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND \leq (V_{IN} or V_{OUT}) \leq V_{CC} . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. 3. V_{IN} from 0.8V to 2.0V

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		UNITS		
TANAMETER	OTHIDOL	▼CC	CONDITIONS	25°C	85°C	FULL RANGE⁴	J.II.
Minimum High-Level	V _{IH}	4.5V	$V_{OUT} = 0.1V \text{ or } V_{CC}$	2	2	2	V
Input Voltage	V IH	5.5V	-0.1V	2	2	2	V
Maximum Low-Level	V	4.5V	$V_{OUT} = 0.1V \text{ or } V_{CC}$	0.8	0.8	0.8	V
Input Voltage	5.5V	-0.1V	0.8	0.8	0.8	V	
Minimum High-Level		4.5V	Ι _{ΟυΤ} = -50μΑ	4.4	4.4	4.4	V
	5.5V	1001 – -30μΑ	5.4	5.4	5.4	V	
Output Voltage	∨он [4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	3.86	3.76	3.76	V
		5.5V	$I_{OH} = -24 \text{mA}$	4.86	4.76	4.76	, v

^{4.} -40° C $\leq T_{J} \leq +85^{\circ}$ C





Rev 1.0 13/05/21

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL V	V _{cc}	V _{CC} CONDITIONS		LIMITS			
	OTHIBOL	• 66	CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS	
		4.5V	I _{OUT} = 50μA	0.1	0.1	0.1	V	
Maximum Low-Level	V _{OL}	5.5V	1001 – 30μΑ	0.1	0.1	0.1	V	
Output Voltage	V OL	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	0.36	0.44	0.44	V	
		5.5V I _{OL} = 24mA	0.36	0.44	0.44	V		
Maximum Input Leakage Current	I _{IN}	5.5V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	μA	
Additional Maximum I _{CC} / Input	ΔI _{CCT}	5.5V	V _{IN} = V _{CC} -2.1V	1	1.5	1.5	mA	
Minimum Dynamic	I _{OLD}	5.5V	V _{OLD} = 1.65V Max	-	75	75	mA	
Output Current ⁶	I _{OHD}	5.5V	V _{OHD} = 3.85V Min	-	-75	-75	ША	
Maximum Quiescent Supply Leakage Current	I _{CC}	5.5V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	40	μА	

^{5.} All outputs loaded; thresholds on input associated with output under test. 6. Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics⁷

PARAMETER	SYMBOL	Vac	V _{cc} CONDITIONS		LIMI	TS	UNITS
TAIVAILLER	OTHEOL	•66		25°C	85°C	FULL RANGE⁴	Oitilo
Propagation Delay Input A,B,C to Output Y	t _{PLH}	5V ±0.5	$C_L = 50pF,$ input $t_r = t_f = 3.0ns$	9.5	10.5	10.5	ns
Propagation Delay Input A,B,C to Output Y	t _{PHL}	5V ±0.5	$C_L = 50pF,$ input $t_r = t_f = 3.0ns$	9.5	10.5	10.5	ns

Capacitance⁷ (V_{cc} = 5V, T_j = 25°C)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS	LIMITS	UNITS
Input Capacitance	C _{IN}	5V	V _{IN} = V _{CC} or GND	4.5	pF
Power Dissipation Capacitance	C _{PD}	5V	C _L = 50pF, f = 1 MHz	TYPICAL 20	pF

^{7.} Not production tested in die form, characterized by chip design and tested in package.





Rev 1.0 13/05/21

Switching Waveform

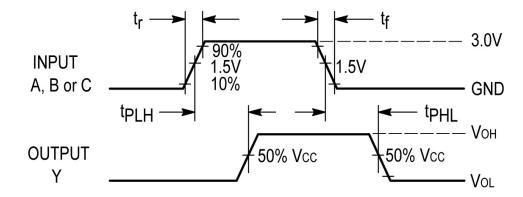
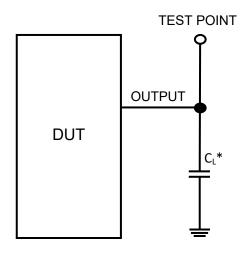


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



^{*} Includes all probe and jig capacitance

Figure 2

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

