

Features:

#### Hex Inverter Gate with LSTTL compatible inputs in bare die form

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#### Description

The 74ACT04 hex inverter gate is fabricated on a 1.5 $\mu$ m advanced 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device contains six independent inverters which perform the Boolean function Y =  $\bar{A}$ . Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are directly compatible with both standard TTL and CMOS outputs. All inputs are protected against ESD and excess voltage transients

### **Ordering Information**

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see 54ACT04

# Die Dimensions in µm (mils)

Inputs directly accept TTL

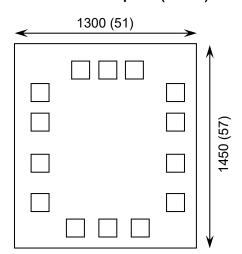
Outputs Source/Sink 24 mA

Low Input Current: 1µA

Outputs directly interface CMOS, NMOS and TTL

Functionally compatible with bipolar 74LS04

Lower power alternative to bipolar logic.



### **Supply Formats:**

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

### **Mechanical Specification**

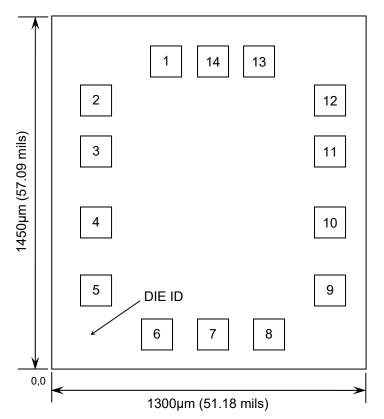
Die Size (Unsawn)	1300 x 1450 51 x 57	µm mils	
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils	
Top Metal Composition	Al 1%Si 1.1μ	m	
Back Metal Composition	ck Metal Composition N/A – Bare Si		





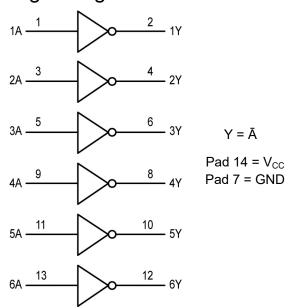
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### Pad Layout and Functions



PAD	FUNCTION	COORDINA	ATES (mm)				
FAD	TONCTION	X	Y				
1	1A	0.410	1.200				
2	1Y	0.120	1.040				
3	2A	0.120	0.830				
4	2Y	0.120	0.540				
5	3A	0.120	0.260				
6	3Y	0.370	0.080				
7	GND	0.600	0.080				
8	4Y	0.830	0.080				
9	4A	1.080	0.260				
10	5Y	1.080	0.540				
11	5A	1.080	0.830				
12	6Y	1.080	1.040				
13	6A	0.790	1.200				
14	V <sub>CC</sub>	0.600	1.200				
CONNECT CHIP BACK TO V <sub>CC</sub> OR FLOAT							

### Logic Diagram



### **Truth Table**

INPUTS	OUTPUT				
Α	Υ				
Н	L				
L	Н				
H = High level (steady state)					
L = Low level (steady state)					





### Absolute Maximum Ratings<sup>1</sup>

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PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V <sub>CC</sub>	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Output Voltage (Referenced to GND)	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Input Current	I <sub>IN</sub>	±20	mA
DC Output Current, per pad	I <sub>OUT</sub>	±50	mA
DC Supply Current, V <sub>CC</sub> or GND, per pad	I <sub>cc</sub>	±50	mA
Power Dissipation in Still Air <sup>2</sup>	P <sub>D</sub>	750	mW
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C

<sup>1.</sup> Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

### Recommended Operating Conditions<sup>3</sup> (Voltages Referenced to GND)

			, ,		,
PARAMETE	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	$V_{CC}$	4.5	5.5	V	
DC Input or Output Voltag	$V_{IN}$ , $V_{OUT}$	0	V <sub>CC</sub>	V	
Operating Temperature Range		T <sub>J</sub>	-40	+85	°C
Output current - High		I <sub>OH</sub>	-	-24	mA
Output current - Low		I <sub>OL</sub>	-	24	mA
Input Rise or Fall rate	V <sub>CC</sub> = 4.5V	Δt/ΔV	0	10	ns/V
(V <sub>IN</sub> from 0.8V to 2V)	V <sub>CC</sub> = 5.5V	ΔυΔν	0	8	115/V

<sup>3.</sup> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

### DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V <sub>cc</sub>	CONDITIONS	LIMITS			LIMITS			UNITS
	OTHEOL	•66	CONDITIONS	25°C	85°C	FULL RANGE⁴	Oiiiio			
Minimum High-Level	V <sub>IH</sub>	4.5V	$V_{OUT} = 0.1V$	2	2	2	V			
Input Voltage	VIH	5.5V	or V <sub>CC</sub> -0.1V	2	2	2	V			
Maximum Low-Level	V <sub>IL</sub>	4.5V	$V_{OUT} = 0.1V$ or $V_{CC}$ -0.1V	0.8	0.8	0.8	V			
Input Voltage	VIL	5.5V		0.8	0.8	0.8				
Minimum Low-Level Output Voltage	-	4.5V	Ι <sub>ΟυΤ</sub> = 50μΑ	0.1	0.1	0.1	V			
		5.5V	1001 – 30μΑ	0.1	0.1	0.1	V			
	▼ OL	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	0.36	0.44	0.44	V			
		5.5V	$I_{OL} = 24mA$	0.36	0.44	0.44	<b>V</b>			

 <sup>-40°</sup>C ≤ T<sub>J</sub> ≤ +85°C
 All outputs loaded; thresholds on input associated with output under test.





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### DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V <sub>cc</sub>	CONDITIONS		UNITS		
	OTHIDOL	STIMBOL VCC CONDITIONS	25°C	85°C	FULL RANGE⁴	ONITO	
		4.5V	Ι <sub>ΟυΤ</sub> = 50μΑ	4.4	4.4	4.4	V
Minimum High-Level	V <sub>OH</sub>	5.5V	1001 – 30μΑ	5.4	5.4	5.4	
Output Voltage	V OH	4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	3.86	3.76	3.76	V
		5.5V	$I_{OH} = -24mA$	4.86	4.76	4.76	V
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Additional Maximum I <sub>CC</sub> / Input	ΔI <sub>CCT</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> -2.1V	0.6	1.5	1.5	mA
Minimum Dynamic	I <sub>OLD</sub>	5.5V	V <sub>OLD</sub> = 1.65V Max	-	75	75	mA
Output Current <sup>6</sup>	I <sub>OHD</sub>	5.5V	V <sub>OHD</sub> = 3.85V Min	-	-75	-75	ША
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	5.5V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	4	40	40	μА

<sup>6.</sup> Maximum test duration 2ms, one output loaded at a time.

## AC Electrical Characteristics<sup>7</sup> V<sub>CC</sub> = 5.0V ±0.5V

PARAMETER	SYMBOL V <sub>cc</sub>	Vac	V <sub>CC</sub> CONDITIONS		UNITS		
	OTHIDOL	OTHIDOL VCC COL		25°C	85°C	FULL RANGE⁴	Oitilo
Maximum Propagation Delay	t <sub>PLH</sub>	5.0V	Input	8.5	9	9	ns
Input A to Output Y (Figure 1)	t <sub>PHL</sub>	5.0V		8	8.5	8.5	
Maximum Input	C <sub>IN</sub>	5.0V	T <sub>J</sub> = 25°C		TYPIC	AL	pF
Capacitance		0.01	3.0V 1J = 23 C		4.5		Pi
Power Dissipation Capacitance	C <sub>PD</sub>	5.0V	$T_J = 25$ °C, $C_L = 50$ pF		30		pF

<sup>7.</sup> Not production tested in die form, characterized by chip design and tested in package.





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### Switching Waveform

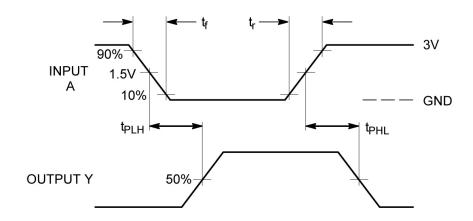
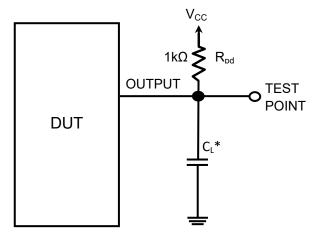


Figure 1 – Propagation delay, Input A to Output Y

#### **Test Circuit**



<sup>\*</sup> Includes all probe and jig capacitance

Figure 2 - Test Circuit

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