

Quad 2-input NOR gates with LSTTL compatible inputs in bare die form

Rev 1.0 18/05/21

Description

The 74ACT02 quad 2-input NOR gate is fabricated on a 1.5µm advanced CMOS process combining high speed LSTTL performance with CMOS low power. The device performs the Boolean function Y = (A + B) or Y = $\overline{A} \cdot \overline{B}$ in positive logic. Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are directly compatible with LSTTL outputs. All inputs are protected against ESD and excess voltage transients.

Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 74LS02
- Lower power alternative to bipolar logic

Ordering Information

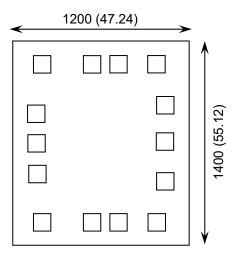
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT02

Die Dimensions in µm (mils)



Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

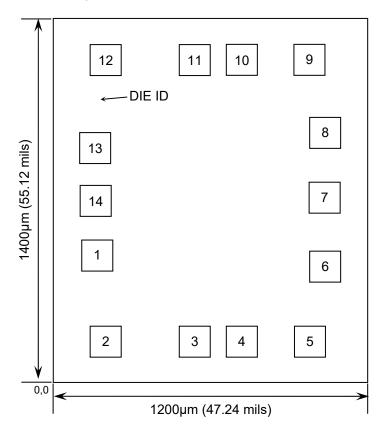
| Die Size (Unsawn) | 1200 x 1400 | μm | |
|-------------------------|---------------|------|--|
| (5.1.5.1.1.7) | 47 x 55 | mils | |
| Minimum Bond Pad Size | 130 x 130 | μm | |
| Willimani Bond Pad Size | 5.12 x 5.12 | mils | |
| Die Thielmese | 350 (±20) | μm | |
| Die Thickness | 13.78 (±0.79) | mils | |
| Top Metal Composition | Al 1%Si 1.1μ | m | |
| Back Metal Composition | N/A – Bare Si | | |





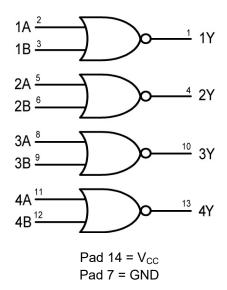
Rev 1.0 18/05/21

Pad Layout and Functions



| PAD | FUNCTION | COORDINA | ATES (mm) | | | | | |
|-----|---|----------|-----------|--|--|--|--|--|
| FAD | TONCTION | X | Υ | | | | | |
| 1 | 1Y | 0.100 | 0.430 | | | | | |
| 2 | 1A | 0.140 | 0.100 | | | | | |
| 3 | 1B | 0.480 | 0.100 | | | | | |
| 4 | 2Y | 0.660 | 0.100 | | | | | |
| 5 | 2A | 0.920 | 0.100 | | | | | |
| 6 | 2B | 0.980 | 0.380 | | | | | |
| 7 | GND | 0.980 | 0.650 | | | | | |
| 8 | 3A | 0.980 | 0.900 | | | | | |
| 9 | 3B | 0.920 | 1.180 | | | | | |
| 10 | 3Y | 0.660 | 1.180 | | | | | |
| 11 | 4A | 0.480 | 1.180 | | | | | |
| 12 | 4B | 0.140 | 1.180 | | | | | |
| 13 | 4Y | 0.100 | 0.840 | | | | | |
| 14 | V _{CC} | 0.140 | 0.640 | | | | | |
| CON | CONNECT CHIP BACK TO V _{CC} OR FLOAT | | | | | | | |

Logic Diagram



Truth Table

| INP | UTS | OUTPUT | | | | | |
|-------------------------------|------------------------------|--------|--|--|--|--|--|
| Α | В | Υ | | | | | |
| L | L | Н | | | | | |
| L | H | L | | | | | |
| Н | L | L | | | | | |
| Н | Н | L | | | | | |
| H = High level (steady state) | | | | | | | |
| L = L | L = Low level (steady state) | | | | | | |





Absolute Maximum Ratings¹

Rev 1.0 18/05/21

| PARAMETER | SYMBOL | VALUE | UNIT |
|--|------------------|------------------------------|------|
| DC Supply Voltage (Referenced to GND) | V _{CC} | -0.5 to +7.0 | V |
| DC Input Voltage (Referenced to GND) | V _{IN} | -0.5 to V _{CC} +0.5 | V |
| DC Output Voltage (Referenced to GND) | V _{OUT} | -0.5 to V _{CC} +0.5 | V |
| DC Input Current | I _{IN} | ±20 | mA |
| DC Output Current, per pad | I _{OUT} | ±50 | mA |
| DC Supply Current, V _{CC} or GND, per pad | I _{CC} | ±50 | mA |
| Power Dissipation in Still Air ² | P _D | 750 | mW |
| Storage Temperature Range | T _{STG} | -65 to 150 | °C |

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages Referenced to GND)

| | | , , | | , |
|--|-----------------------------------|-----|-----------------|--------|
| PARAMETER | SYMBOL | MIN | MAX | UNITS |
| DC Supply Voltage | V _{CC} | 4.5 | 5.5 | V |
| DC Input or Output Voltage | V _{IN} ,V _{OUT} | 0 | V _{CC} | V |
| Operating Temperature Range | TJ | -40 | +85 | °C |
| Output current - High | I _{OH} | - | -24 | mA |
| Output current - Low | I _{OL} | - | 24 | mA |
| Input Rise or Fall rate V _{CC} = 4.5V | Δt/ΔV | 0 | 10 | ns/V |
| $(V_{IN} \text{ from 0.8V to 2V})$ $V_{CC} = 5.5V$ | ΔυΔν | 0 | 8 | 115/ V |

^{3.} This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

| PARAMETER | SYMBOL | SYMBOL V _{CC} CONDI | | DITIONS | | LIMITS | | |
|----------------------------------|-----------------|--|--|---------|------|-------------|-------|--|
| TAKAMETER | OTHIBOL | ▼ CC | CONDITIONS | 25°C | 85°C | FULL RANGE⁴ | UNITS | |
| Minimum High-Level | V _{IH} | 4.5V | $V_{OUT} = 0.1V$ | 2 | 2 | 2 | V | |
| Input Voltage | VIH | 5.5V | or V _{CC} -0.1V | 2 | 2 | 2 | V | |
| Maximum Low-Level | V _{IL} | 4.5V | $V_{OUT} = 0.1V$ | 0.8 | 8.0 | 0.8 | V | |
| Input Voltage | V IL | 5.5V | or V _{CC} -0.1V | 0.8 | 8.0 | 0.8 | V | |
| Minimum Low-Level Output Voltage | | 4.5V | I _{OUT} = 50μA | 0.1 | 0.1 | 0.1 | V | |
| | | 5.5V | | 0.1 | 0.1 | 0.1 | | |
| | 4.5V | $V_{IN} = V_{IL} \text{ or } V_{IH}^5$ | 0.36 | 0.44 | 0.44 | V | | |
| | 5.5V | 5.5V | $I_{OL} = 24mA$ | 0.36 | 0.44 | 0.44 | V | |
| | | 4.5V | $V_{IN} = V_{IL} \text{ or } V_{IH}^{5,6}$ | - | - | 1.65 | V | |
| | 5.5 | 5.5V | $I_{OL} = 75mA$ | - | - | 1.65 | \ \ \ | |

^{4. -40°}C ≤ T_J ≤ +85°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 85°C





Rev 1.0 18/05/21

DC Electrical Characteristics Continued (Voltages referenced to GND)

| PARAMETER | SYMBOL | V _{cc} CONDITIONS | | | UNITS | | |
|--|-------------------|----------------------------|---|------|-------|-------------|--------|
| | OTHIDOL | IBOL Vec GONDING | CONDITIONS | 25°C | 85°C | FULL RANGE⁴ | Oitilo |
| | | 4.5V | I _{OUT} = 50μA | 4.4 | 4.4 | 4.4 | V |
| Minimum High-Level | V _{OH} | 5.5V | 1001 – 30μΛ | 5.4 | 5.4 | 5.4 | V |
| Output Voltage | V OH | 4.5V | $V_{IN} = V_{IL} \text{ or } V_{IH}^5$ | 3.86 | 3.76 | 3.76 | V |
| | | 5.5V | $I_{OH} = -24mA$ | 4.86 | 4.76 | 4.76 | V |
| Maximum Input Leakage Current | I _{IN} | 5.5V | V _{IN} = V _{CC} or GND | ±0.1 | ±1.0 | ±1.0 | μA |
| Additional Maximum I _{CC} / Input | ΔI _{CCT} | 5.5V | V _{IN} = V _{CC} -2.1V | 0.6 | 1.5 | 1.5 | mA |
| Minimum Dynamic | I _{OLD} | 5.5V | V _{OLD} = 1.65V Max | - | 75 | 75 | mA |
| Output Current ⁷ | I _{OHD} | 5.5V | V _{OHD} = 3.85V Min | - | -75 | -75 | 111/4 |
| Maximum Quiescent Supply Leakage Current | I _{CC} | 5.5V | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$ | 4 | 40 | 40 | μА |

^{7.} Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics 8 $V_{cc} = 5.0V \pm 0.5V$

| PARAMETER | SYMBOL | SYMBOL V _{cc} | V _{cc} CONDITIONS | | UNITS | | |
|-----------------------------------|------------------|------------------------|---------------------------------|------|-------|-------------|----|
| | OTHIDOL | • 66 | CONDITIONS | 25°C | 85°C | FULL RANGE⁴ | |
| Maximum Propagation Delay | t _{PLH} | 5.0V | C _L = 50pF, | 8.5 | 9 | 9 | ns |
| Input A to Output Y (Figure 1) | t _{PHL} | 5.0V | 4. 46. 0.0 | 9.5 | 10 | 10 | |
| Maximum Input | C _{IN} | 5.0V | T _J = 25°C | | TYPIC | AL | pF |
| Capacitance | JIN 0.01 | 0.50 | 1,5 25 5 | | 4.5 | | Pi |
| Power Dissipation Capacitance | C _{PD} | 5.0V | $T_J = 25$ °C, $C_L = 50$ pF | | 30 | | pF |

^{8.} Not production tested in die form, characterized by chip design





Rev 1.0 18/05/21

Switching Waveform

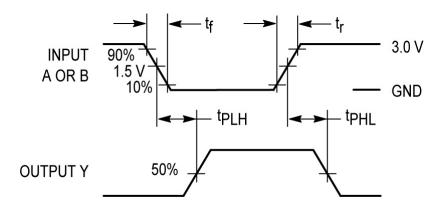
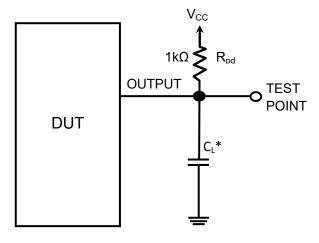


Figure 1 – Propagation delay, Input A or B to Output Y

Test Circuit



^{*} Includes all probe and jig capacitance

Figure 2 - Test Circuit

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