Advanced CMOS Logic – 74AC273

8-bit D-Type Flip-Flop with common reset and clock inputs in bare die form

Rev 1.0
07/12/2021

Description

The 74AC273 consists of eight D-type flip-flops fabricated using a 1.5µm 5V CMOS process combining high speed performance LSTTL performance with CMOS low power consumption. Each flip-flop is equipped with buffered common Clock (CP) and common Reset ($\overline{MR}$) inputs. A low-to-high clock transition loads each flip-flop. Reset is asynchronous and enabled with active low. Inputs accept standard CMOS outputs or LSTTL outputs using pull-up resistors. Inputs are also equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Buffered common clock
- Buffered asynchronous master reset
- Outputs Source/Sink 24mA
- Low input current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating voltage range: 2.0V to 6.0V
- Function compatible with 74HC273.

Ordering Information

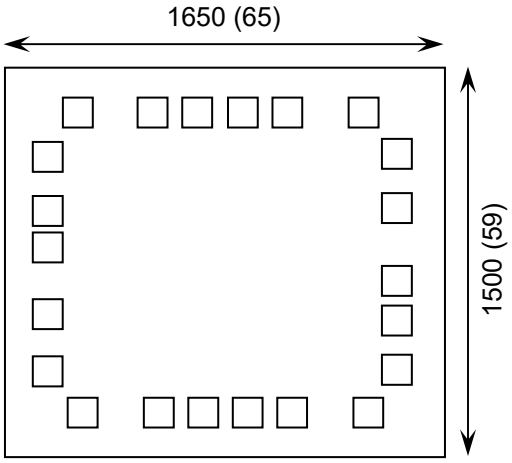
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54AC273

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 460µm(18 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1650 x 1500 65 x 59	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	460 (±20) 18.11 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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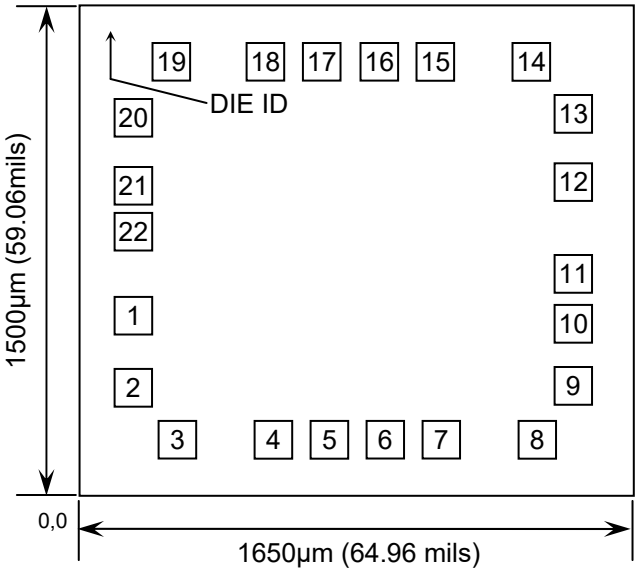
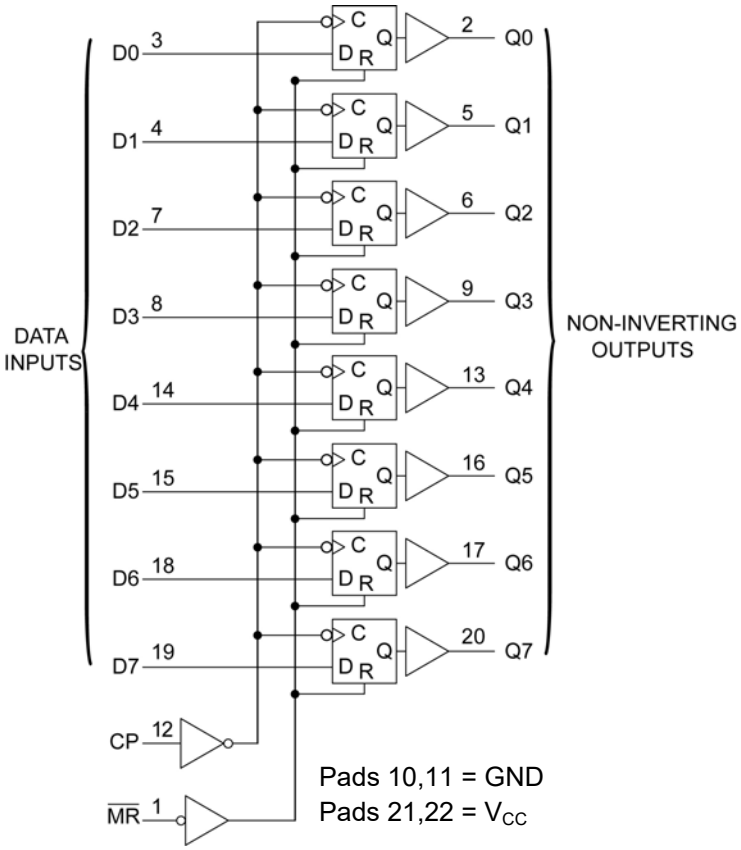
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{MR}$	0.120	0.507
2	Q0	0.117	0.286
3	D0	0.247	0.127
4	D1	0.531	0.127
5	Q1	0.699	0.127
6	Q2	0.867	0.127
7	D2	1.035	0.127
8	D3	1.318	0.127
9	Q3	1.426	0.294
10	GND	1.426	0.483
11	GND	1.426	0.570
12	CP	1.428	0.900
13	Q4	1.426	1.120
14	D4	1.299	1.279
15	D5	1.015	1.279
16	Q5	0.847	1.279
17	Q6	0.679	1.279
18	D6	0.511	1.279
19	D7	0.228	1.279
20	Q7	0.117	1.111
21	V_{CC}	0.117	0.903
22	V_{CC}	0.117	0.816
CONNECT CHIP BACK TO V_{CC}			

Logic Diagram



Truth Table

INPUTS			OUTPUT
$\overline{MR}$	CP	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change
H	↓	X	No Change

H = High level (steady state)
L = Low level (steady state)
X = Don't care

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2.0	6.0	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-40	+85	°C
Output current - High		I_{OH}	-	-24	mA
Output current - Low		I_{OL}	-	24	mA
Input Rise or Fall rate (V_{IN} from 30% to 70% V_{CC})	V_{CC} = 3.0V	Δt/ΔV	0	150	ns/V
	V_{CC} = 4.5V		0	40	
	V_{CC} = 5.5V		0	25	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	3.0V	V_{OUT} = 0.1V or V_{CC} -0.1V	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V_{IL}	3.0V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.9	0.9	0.9	V
		4.5V		1.35	1.35	1.35	
		5.5V		1.65	1.65	1.65	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	3.0V	$I_{OUT} \le -50\mu A$	2.9	2.9	2.9	V
		4.5V		4.4	4.4	4.4	
		5.5V		5.4	5.4	5.4	
		3.0V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA	2.56	2.46	2.46	
		4.5V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24mA$[5]	3.86	3.76	3.76	
		5.5V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24mA$[5]	4.86	4.76	4.76	
		5.5V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -75mA$[6]	-	-	3.85	
Maximum Low-Level Output Voltage	V_{OL}	3.0V	$I_{OUT} = 50\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		5.5V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 12mA$	0.36	0.44	0.44	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 24mA$[5]	0.36	0.44	0.44	
		5.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 24mA$[5]	0.36	0.44	0.44	
		5.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert$ 75mA[6]	-	-	-	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Minimum Dynamic Output Current[7]	I_{OLD}	5.5V	$V_{OLD} = 1.65V$ Max	-	75	75	mA
	I_{OHD}	5.5V	$V_{OHD} = 3.85V$ Min	-	-75	-75	
Maximum Quiescent Supply Current	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	8	80	80	µA

5. All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 85°C **7.** Maximum test duration 2ms, one output loaded at a time

AC Electrical Characteristics[8] (V_{CC} 3.3V ±0.3V, V_{CC} 5V ±0.3V)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Clock Frequency (Figure 1)	f_{max}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	90	75	75	MHz
		5.0V		140	125	125	
Maximum Propagation Delay CP to Q (Figure 1)	t_{PLH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	12.5	14.0	14.0	ns
		5.0V		9.0	10.0	10.0	
	t_{PHL}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	13.0	14.5	14.5	ns
		5.0V		10.0	11.0	11.0	
Maximum Propagation Delay MR to Q (Figure 2)	t_{PLH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	13.0	14.0	14.0	ns
		5.0V		10.0	10.5	10.5	
	t_{PHL}	3.3V		12.0	14.0	14.0	ns
		5.0V		8.5	10.0	10.0	
Maximum Input Capacitance	C_{IN}	-	-	4.5	4.5	4.5	pF
Power Dissipation Capacitance[9]	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			
				50			pF

8. Not production tested in die form, characterized by chip design.
9. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[6] (V_{CC} 3.3V ±0.3V, V_{CC} 5V ±0.3V)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to CP (Figure 3)	t_{SU}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	5.5	6.0	6.0	ns
		5V		4.0	4.5	4.5	
Minimum Hold Time, D to CP (Figure 3)	t_h	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	0	0	0	ns
		5V		1.0	1.0	1.0	
Minimum Pulse Width, CP (Figure 1)	t_w	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	5.5	6.0	6.0	ns
		5V		4.0	4.5	4.5	
Minimum Pulse Width, MR (Figure 2)	t_w	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	5.5	6.0	6.0	ns
		5V		4.0	4.5	4.5	
Minimum Recovery Time, MR to CP (Figure 2)	t_{rec}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	3.5	4.5	4.5	ns
		5V		2.0	3.0	3.0	

Switching Waveforms

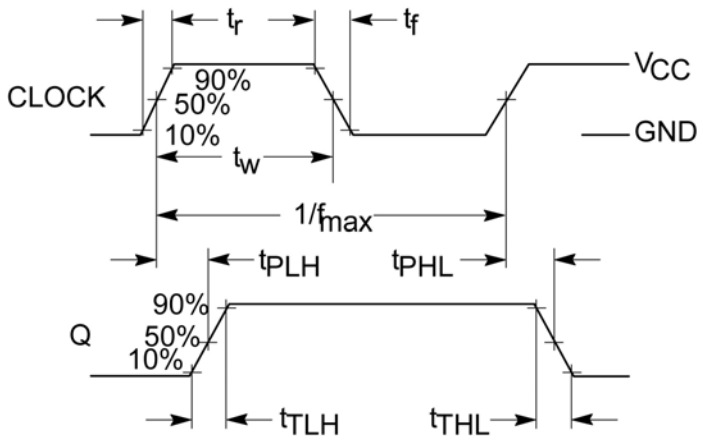


Figure 1 – Propagation Delay & Output Transition Time

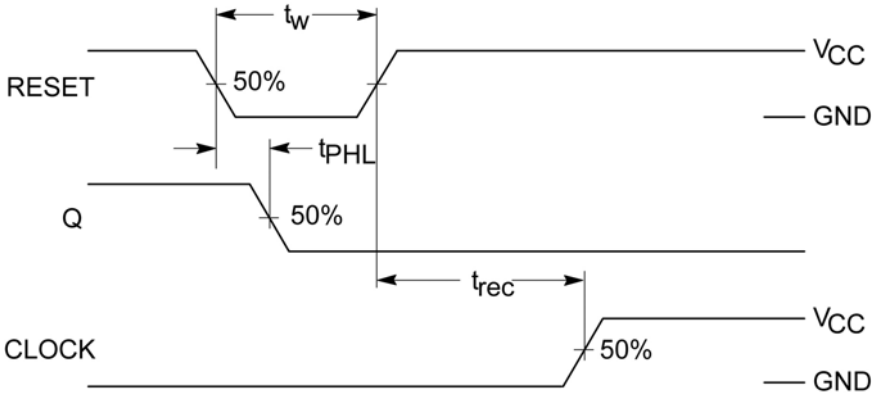


Figure 2 – Propagation Delay – Reset to Q

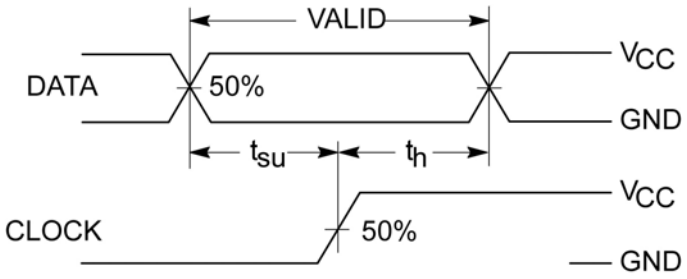
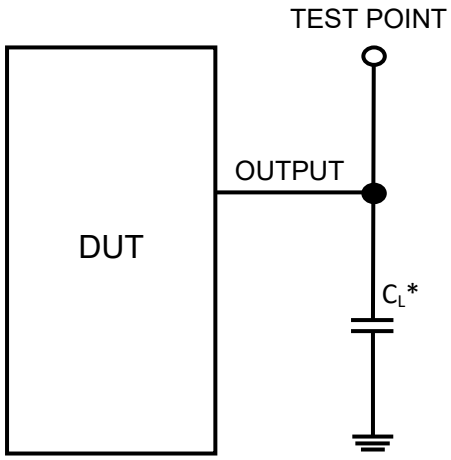


Figure 3 – Timing Requirements

Test Circuit



* Includes all probe and jig capacitance

Figure 4