Very High Speed CMOS Logic - 54VHC373

8-bit transparent D-Type Latch with 3-State Outputs in bare die form

Rev 1.0
26/09/20

Description

The 54VHC373 consists of eight D-type transparent latches fabricated using a 1.5µm 5V advanced CMOS process to combine high speed performance LSTTL performance with CMOS low power consumption. Each latch is equipped with separate D-Type inputs and 3-State outputs for bus oriented applications. Data output changes asynchronously and data may be latched even when the outputs are not enabled. Device inputs accept standard CMOS outputs or LSTTL outputs using pull-up resistors. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- High Speed: t_{PD} = 7.2ns (MAX) V_{CC} = 5V
- Outputs Sink/Source 8mA
- Outputs directly interface CMOS, NMOS and TTL
- Low Input Current: 1µA
- Operating Voltage Range: 2V to 5.5V
- Replacement for 54HC373, 54AC373, 54AHC373
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

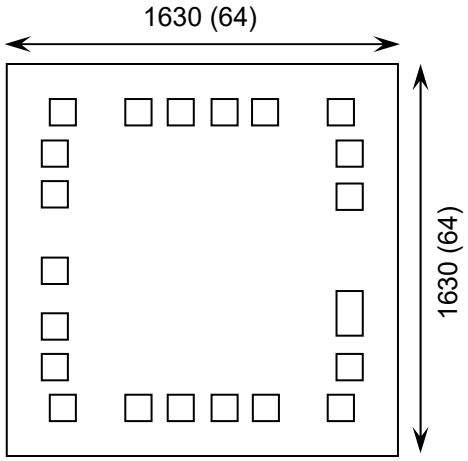
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1630 x 1630 64 x 64	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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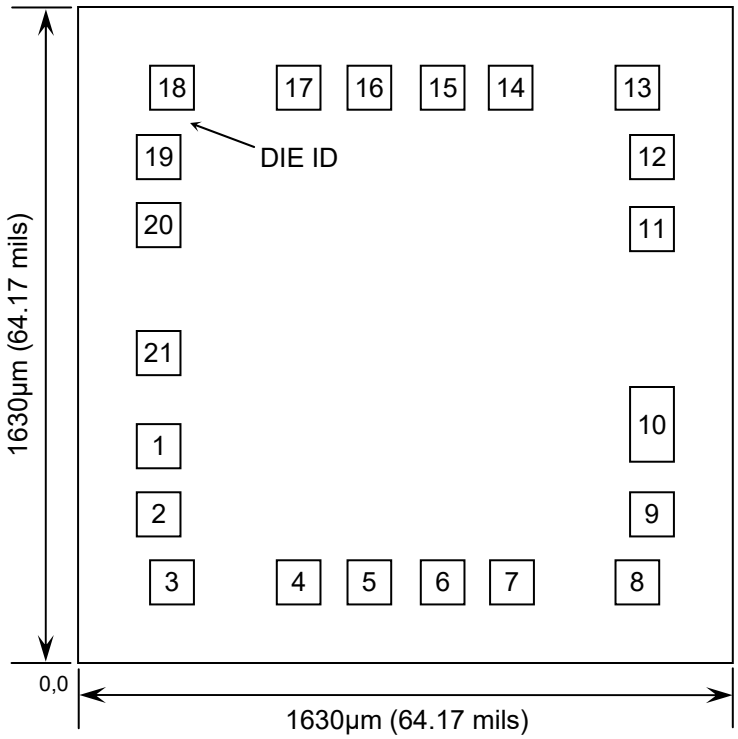
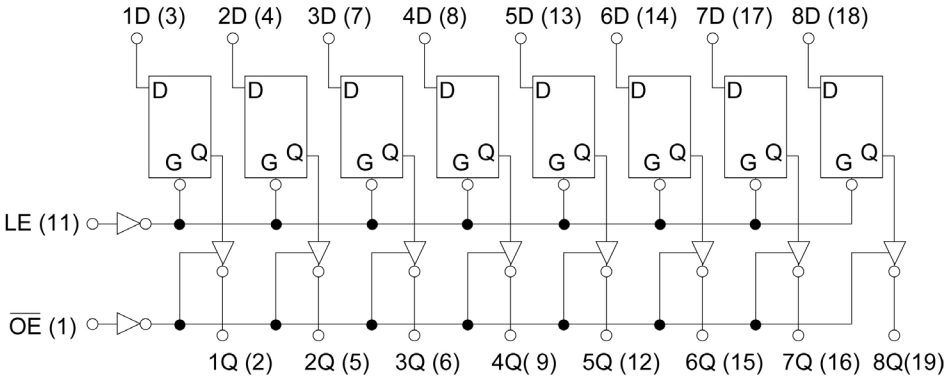
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{OE}$	0.149	0.489
2	1Q	0.149	0.319
3	1D	0.182	0.149
4	2D	0.498	0.149
5	2Q	0.674	0.149
6	3Q	0.855	0.149
7	3D	1.025	0.149
8	4D	1.341	0.149
9	4Q	1.379	0.319
10	GND	1.379	0.499
11	LE	1.379	1.0275
12	5Q	1.379	1.2085
13	5D	1.341	1.3785
14	6D	1.025	1.3785
15	6Q	0.855	1.3785
16	7Q	0.674	1.3785
17	7D	0.498	1.3785
18	8D	0.182	1.3785
19	8Q	0.149	1.2085
20	V_{CC}	0.149	1.0385
21	V_{CC}	0.149	0.722
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 10 = GND, Pad 20 & 21 = V_{CC}

Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance
X = Don't care

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to +7.0	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±75	mA
Power Dissipation in Still Air[2]	P_D	180	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	5.5	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Output Current		I_{OUT}	-	±8	mA
Input Rise and Fall Time	V_{CC} = 3.3V	t_r, t_f	0	100	ns/V
	V_{CC} = 5.5V		0	20	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\|$ ≤ 20μA	1.50	1.50	1.50	V
		3.0V		2.10	2.10	2.10	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\|$ ≤ 20μA	0.50	0.50	0.50	V
		3.0V		0.90	0.90	0.90	
		5.5V		1.65	1.65	1.65	
Minimum High-Level Output Voltage	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ -50μA	1.92	1.90	1.90	V
		3.0V		2.92	2.90	2.90	
		4.5V		4.42	4.40	4.40	
		5.5V		5.52	5.40	5.40	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ -4mA	2.58	2.48	2.40	
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ -8mA	3.94	3.80	3.70	

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert = 50\mu A$	0.09	0.10	0.10	V
		3.0V		0.09	0.10	0.10	
		4.5V		0.09	0.10	0.10	
		5.5V		0.09	0.10	0.10	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert = 4mA$	0.36	0.44	0.50	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert = 8mA$	0.36	0.44	0.50	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±2.0	µA
Maximum 3-State Leakage Current	I_{OZ}	5.5V	High Z Output, $V_{IN} = V_{IL}$ or V_{IH}, $V_{OUT}=V_{CC}$ or GND	±0.25	±2.5	±10	µA
Maximum Quiescent Supply Leakage Current[4]	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \le 0\mu A$	4	40	80	µA

4. $-55^{\circ}C \le T_J \le +125^{\circ}C$

AC Electrical Characteristics[5] V_{CC} = 5.0V ±0.5V, Input $t_r = t_f$ = 3ns, R_L = 1kΩ

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, D to Q, (Figure 1,5)	t_{PLH}, t_{PHL}	3.3V ±10%	C_L = 15pF	11.4	13.5	14.5	ns
			C_L = 50pF	14.9	17.0	19.0	
		5V ±10%	C_L = 15pF	7.2	8.5	9.0	
			C_L = 50pF	9.2	10.5	11.5	
Maximum Propagation Delay, LE to Q, (Figure 2,5)	t_{PLH}, t_{PHL}	3.3V ±10%	C_L = 15pF	11.0	13.0	14.0	ns
			C_L = 50pF	14.5	16.5	18.5	
		5V ±10%	C_L = 15pF	7.2	8.5	9.0	
			C_L = 50pF	9.2	10.5	11.5	
Maximum Propagation Delay, $\overline{OE}$ to Q, (Figure 3,6)	t_{PLZ}, t_{PHZ}	3.3V ±10%	C_L = 50pF	13.2	15.0	17.0	ns
		5V ±10%		9.2	10.5	11.5	
Maximum Propagation Delay, $\overline{OE}$ to Q, (Figure 3,6)	t_{PZL}, t_{PZH}	3.3V ±10%	C_L = 15pF	11.4	13.5	14.5	ns
			C_L = 50pF	14.9	17.0	19.0	
		5V ±10%	C_L = 15pF	8.1	9.5	10.5	
			C_L = 50pF	10.1	11.5	13.0	

5. Not production tested in die form, characterized by chip design.

AC Electrical Characteristics continued[6] V_{CC} = 5.0V ±0.5V, R_L = 1kΩ, Input $t_r = t_f$ = 3ns

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Capacitance	C_{IN}	5V ±10%	C_L = 50pF	10	10	10	pF
Maximum 3-State Output Capacitance	C_{OUT}	5V ±10%	C_L = 50pF	12	12	12	pF
Power Dissipation Capacitance[7]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	LIMITS			pF
				54			

6. Not production tested in die form, characterized by chip design.
7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to LE (Figure 4)	t_{SU}	3.3V ±10%	C_L = 15pF	4.0	4.0	4.0	ns
			C_L = 50pF	4.0	4.0	4.0	
		5V ±10%	C_L = 15pF	4.0	4.0	4.0	
			C_L = 50pF	4.0	4.0	4.0	
Minimum Hold Time, LE to D (Figure 4)	t_h	3.3V ±10%	C_L = 15pF	1.0	1.0	1.0	ns
			C_L = 50pF	1.0	1.0	1.0	
		5V ±10%	C_L = 15pF	1.0	1.0	1.0	
			C_L = 50pF	1.0	1.0	1.0	
Minimum Pulse Width, LE (Figure 4)	t_w	3.3V ±10%	C_L = 15pF	5.0	5.0	5.0	ns
			C_L = 50pF	5.0	5.0	5.0	
		5V ±10%	C_L = 15pF	5.0	5.0	5.0	
			C_L = 50pF	5.0	5.0	5.0	
Propagation delay difference between outputs	t_{OSLH},t_{OSHL}	3.3V ±10%	C_L = 50pF	1.5	1.5	1.5	ns
		5V ±10%		1.0	1.0	1.0	

Noise Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Positive noise of low output voltage	V_{OLP}	5.0	-	0.9	0.9	0.9	V
Negative noise of low output voltage	V_{OLV}	5.0	-	-0.9	-0.9	-0.9	V
Input dynamic high voltage	V_{IHD}	5.0	-	3.5	3.5	3.5	V
Input dynamic low voltage	V_{ILD}	5.0	-	1.5	1.5	1.5	V

Switching Waveforms

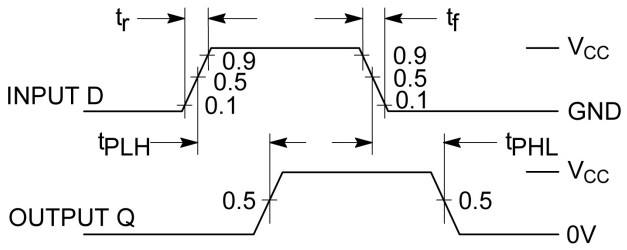


Figure 1 – Propagation Delay & Output Transition Time

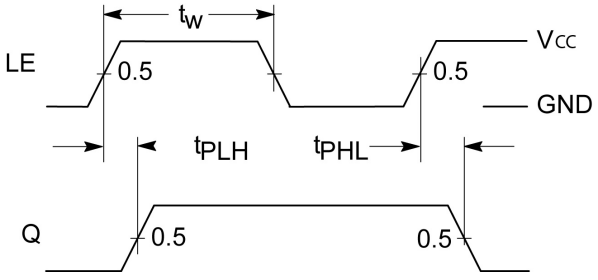


Figure 2 – Propagation Delay – Latch Enable to Q

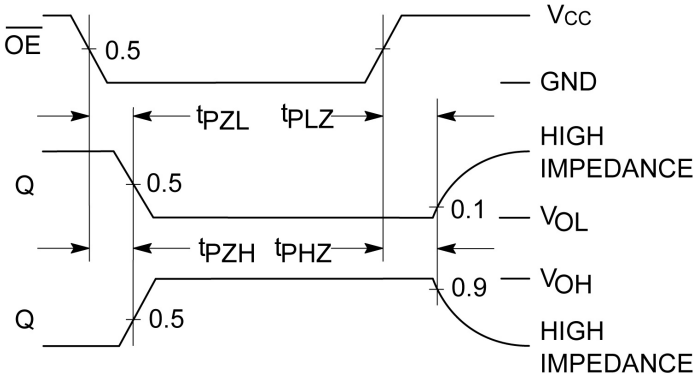


Figure 3 – Propagation Delay - Output Enable to Q

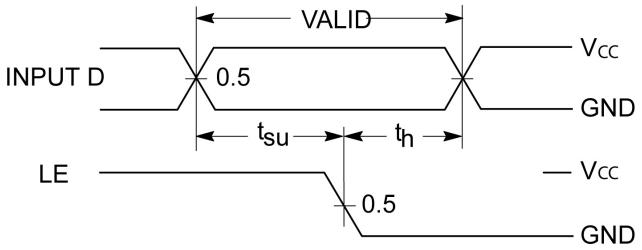
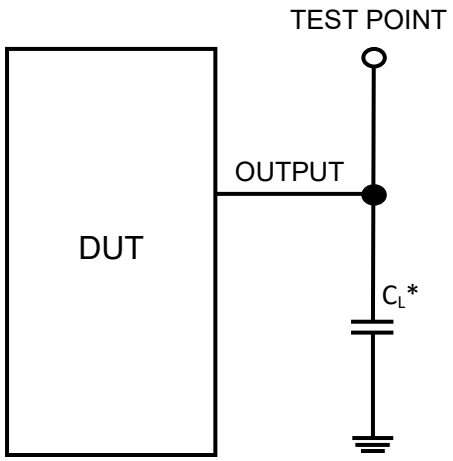


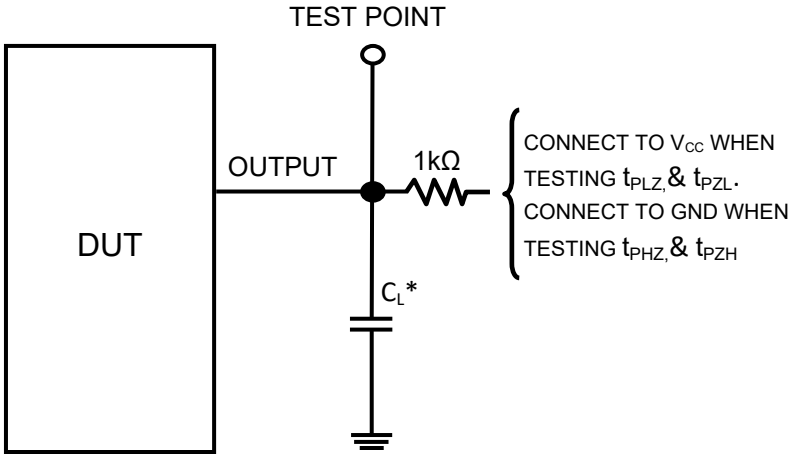
Figure 4 – Timing Requirements

Test Circuits



* Includes all probe and jig capacitance

Figure 5



* Includes all probe and jig capacitance

Figure 6