



# Low Voltage CMOS Logic – 54LVU04

## Low Voltage CMOS Un-buffered Hex Inverter in bare die form

Rev 1.0  
27/07/19

### Description

The 54LVU04 Hex Inverter consists of six independent inverter gates performing the Boolean function  $Y = \bar{A}$  in positive logic. The device is an upgraded replacement for industry standard 54HCU04 and is optimised for low voltage operation. Device inputs are compatible with standard CMOS outputs and also accept TTL directly with a supply between 2.7 and 3.6V. Un-buffered outputs produce lower linear gain for increased compatibility + reliability in crystal oscillator related applications. All inputs are protected against ESD and excess voltage transients.

### Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Inputs directly accept TTL ( $V_{CC}$  2.7V - 3.6V)
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 1V to 5.5V
- Improved direct replacement for 54HCU04
- High Noise Immunity CMOS process.

### Ordering Information

The following part suffixes apply:

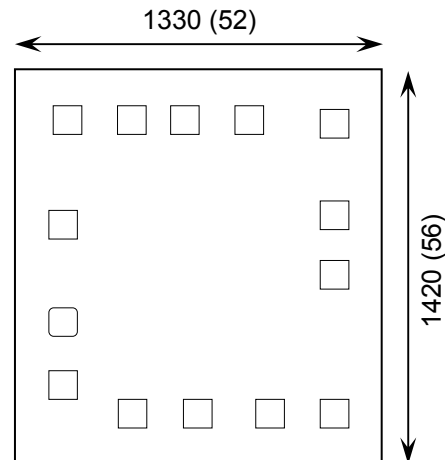
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unsawn)	1330 x 1420 52 x 56	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

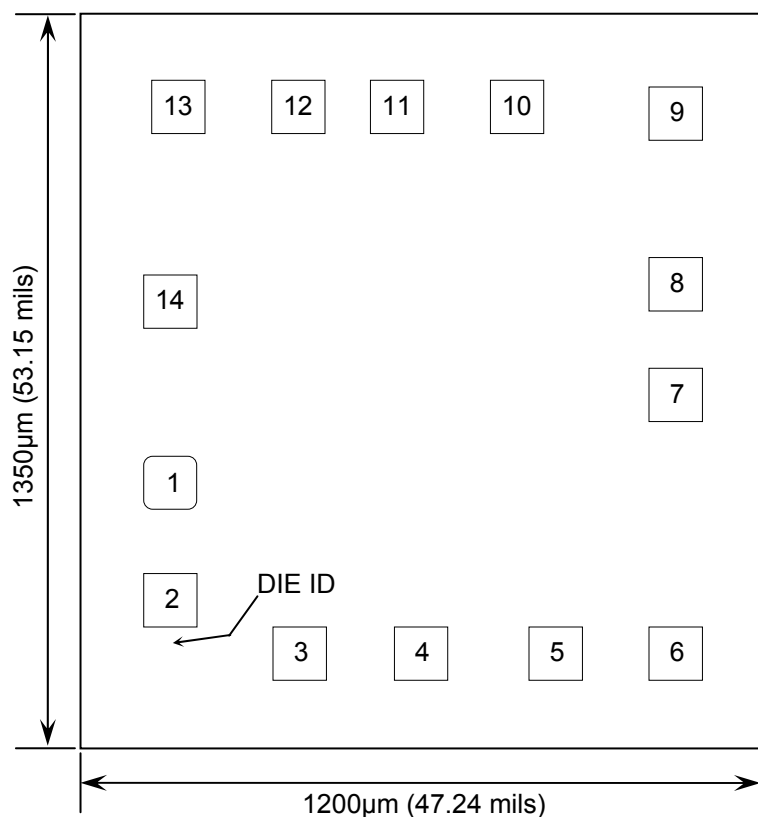




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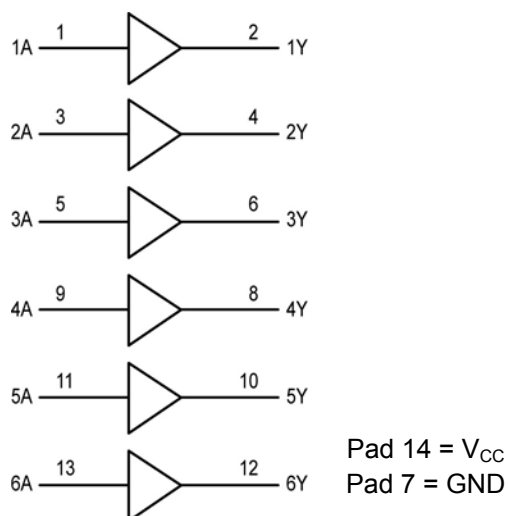
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.130	0.463
2	1Y	0.130	0.230
3	2A	0.381	0.126
4	2Y	0.616	0.126
5	3A	0.881	0.126
6	3Y	1.116	0.126
7	GND	1.115	0.631
8	4Y	1.115	0.846
9	4A	1.115	1.181
10	5Y	0.804	1.194
11	5A	0.569	1.194
12	6Y	0.378	1.194
13	6A	0.143	1.194
14	V <sub>CC</sub>	0.130	0.813

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

## Logic Diagram



## Truth Table

INPUTS	OUTPUT
A	Y
H	L
L	H

H = High level (steady state)  
L = Low level (steady state)





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	$I_{IN}$	±20	mA
DC Output Current, per pad	$I_{OUT}$	±50	mA
DC Supply Current, $V_{CC}$ or GND, per pad	$I_{CC}$	±50	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
Supply Voltage	$V_{CC}$	1	5.5	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	-55	+125	°C	
Input Rise or Fall Times	$t_r, t_f$	$V_{CC} = 1V \leq V_{CC} < 2V$	0	500	ns
		$V_{CC} = 2V \leq V_{CC} < 2.7V$	0	200	
		$V_{CC} = 2.7V \leq V_{CC} < 3.6V$	0	100	
		$V_{CC} = 3.6V \leq V_{CC} < 5.5V$	0	50	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	$V_{CC}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	$V_{IH}$	1.2V	$V_{OUT} = 0.1V \text{ or } V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	1.0	1.0	1.0	V
		2.0V		1.6	1.6	1.6	
		2.7V		2.4	2.4	2.4	
		3.0V		2.4	2.4	2.4	
		3.6V		2.4	2.4	2.4	
		4.5V		3.6	3.6	3.6	
		5.5V		4.4	4.4	4.4	

4.  $-55^\circ C \leq T_J \leq +125^\circ C$





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## DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum Low-Level Input Voltage	V <sub>IL</sub>	1.2V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> -0.1V  I <sub>OUT</sub>   ≤ 20μA	0.2	0.2	0.2	V
		2.0V		0.4	0.4	0.4	
		2.7V		0.5	0.5	0.5	
		3.0V		0.5	0.5	0.5	
		3.6V		0.5	0.5	0.5	
		4.5V		0.9	0.9	0.9	
		5.5V		1.1	1.1	1.1	
Minimum High-Level Output Voltage	V <sub>OH</sub>	1.2V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 100μA	1.05	1.0	1.0	V
		2.0V		1.85	1.8	1.8	
		2.7V		2.55	2.5	2.5	
		3.0V		2.85	2.8	2.8	
		3.6V		3.45	3.4	3.4	
		4.5V		4.35	4.3	4.3	
		5.5V		5.35	5.3	5.3	
	3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6mA	2.48	2.40	2.20	V	
	4.5V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 12mA	3.70	3.60	3.50		
	Maximum Low-Level Output Voltage	V <sub>OL</sub>	1.2V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 100μA	0.15	0.2	0.2
2.0V			0.15		0.2	0.2	
2.7V			0.15		0.2	0.2	
3.0V			0.15		0.2	0.2	
3.6V			0.15		0.2	0.2	
4.5V			0.15		0.2	0.2	
5.5V			0.15		0.2	0.2	
3.0V		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6mA	0.33	0.40	0.50	V	
4.5V		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 12mA	0.40	0.55	0.65		
Maximum Input Leakage Current		I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0μA	4	20	40	μA

4. -55°C ≤ T<sub>J</sub> ≤ +125°C





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## AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Input A or B to Output Y (Figure 1,2)	t <sub>PLH</sub> , t <sub>PHL</sub>	1.2V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 2.5ns R <sub>L</sub> = 1kΩ	70	80	100	ns
		2.0V		22	26	31	
		2.7V		16	19	23	
		3.0V		13	15	18	
		4.5V		11	13	16	
Maximum Input Capacitance	C <sub>IN</sub>	5.5V	-	7	7	7	pF
Power Dissipation Capacitance, Per Inverter <sup>6</sup>	C <sub>PD</sub>	5.5V	T <sub>J</sub> = 25°C, V <sub>IN</sub> = GND or V <sub>CC</sub>	TYPICAL			pF
				36			

5. Not production tested in die form, characterized by chip design and tested in package.

6. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

## Switching Waveform

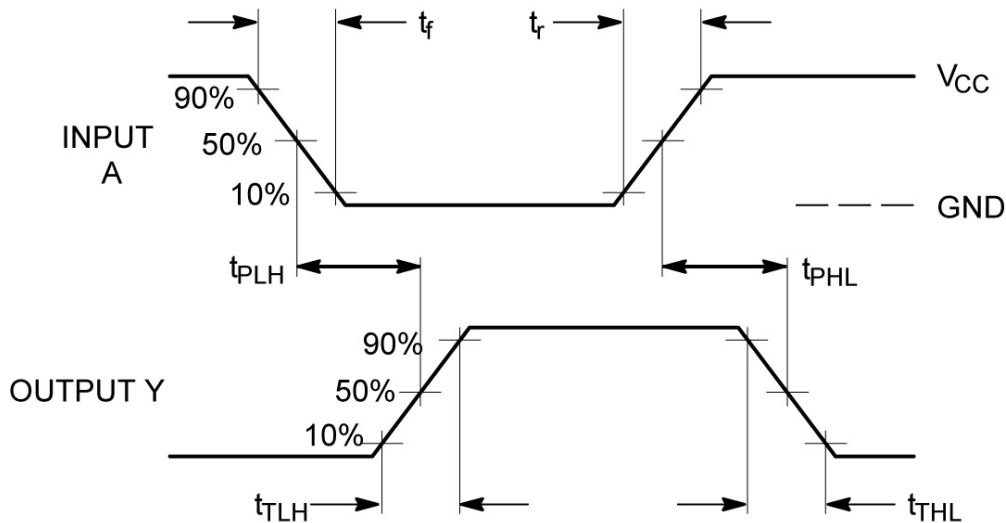


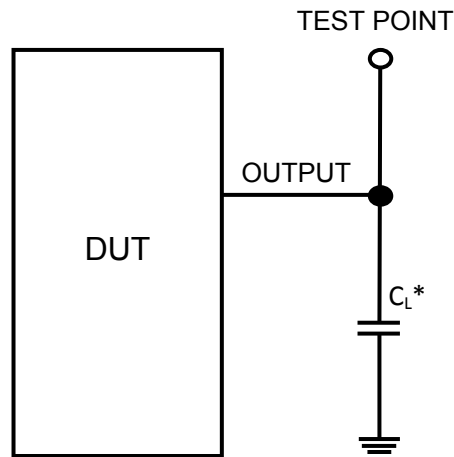
Figure 1 – Propagation Delay & Output Transition Time





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## Test Circuit



\* Includes all probe and jig capacitance

**Figure 2**

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