Low Voltage CMOS Logic – 54LVC2G66

Dual SPST Bilateral Analog Switch in bare die form

Rev 1.0
29/06/19

Description

The 54LVC2G66 Dual Single-Pole Single-Throw Analog Switch is produced using an optimised low voltage CMOS process. Each switch consists of two input/output pins and an active HIGH enable input pin (OE). A LOW signal on the enable pin (OE) turns the analog switch off. Schmitt trigger action on the enable inputs provides circuit tolerance for slow input rise and fall times. Both analog and digital signals are supported in both directions across the full V_{CC} range. The device is suited for multiplexing in analog-to-digital or digital-to-analog conversion and also finds use in signal gating, chopping or modulation/de-modulation applications.

Features:

- Wide supply voltage: V_{CC} 1.65V - 5.5V
- Very low r_{ON} : 6Ω Typ, V_{CC} = 4.5V
- High speed: t_{pd} 0.8ns Max, V_{CC} = 3.3V
- Switch current capability: 32mA
- TTL input compatibility (V_{CC} = 3.3V)
- Enable inputs accept up to 5.5V
- Rail-to-Rail Input / Output
- High noise immunity
- Tiny Die size.

Ordering Information

The following part suffixes apply:

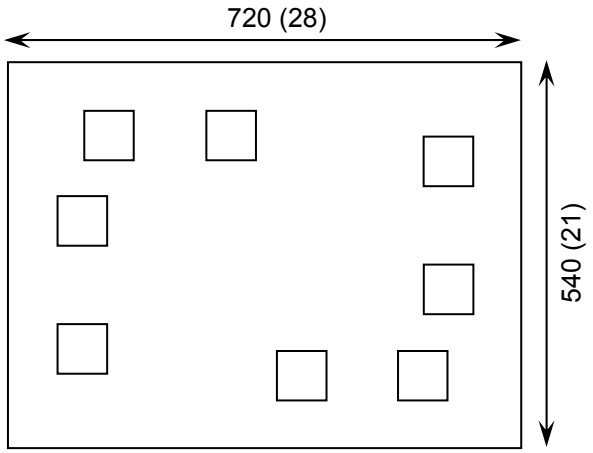
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	720 x 540 28 x 21	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±20) 11.02 (±0.79)	µm mils
Top Metal Composition	Al-Si-Cu 3 µm	
Back Metal Composition	N/A – Bare Si	

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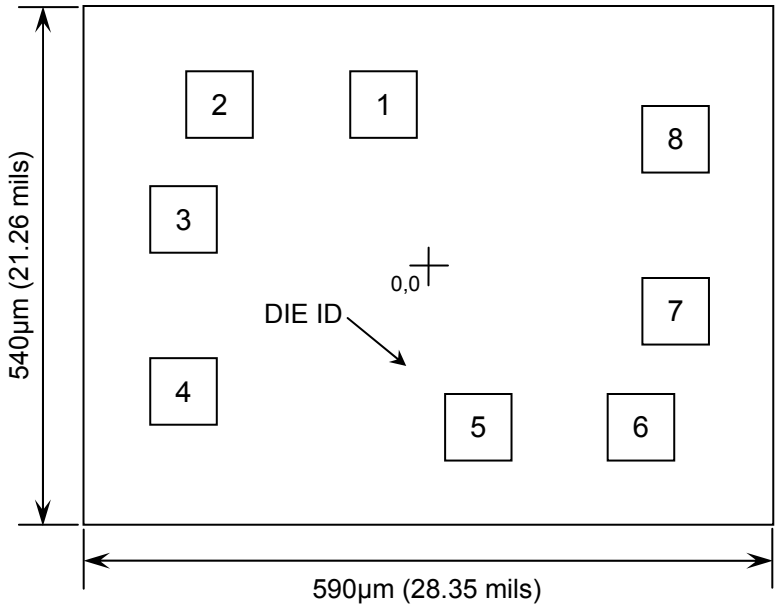
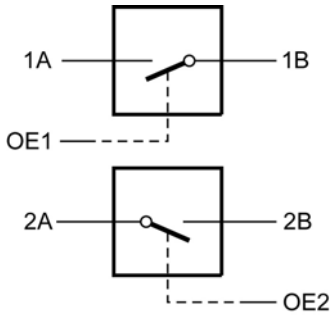
Pad Layout and Functions

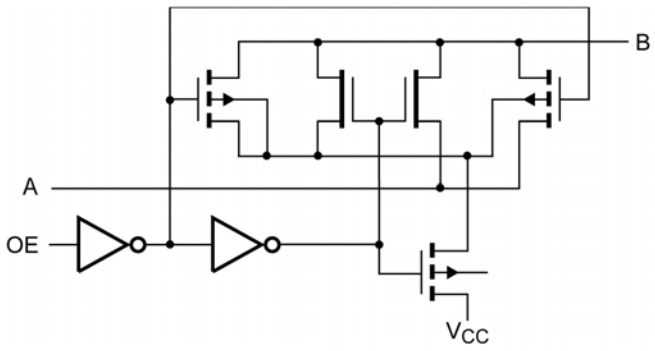


PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	2B	-47.6	166.7
2	OE1	-217.6	166.7
3	V_{CC}	-256.7	47
4	1A	-256.7	-131
5	1B	47.6	-166.7
6	OE2	217.6	-166.7
7	GND	256.4	-47
8	2A	256.7	131
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Expanded Logic Diagram (x1 Switch)



Function Table

OE	SWITCH
H	ON
L	OFF
H = High level (steady state) L = Low level (steady state)	

Absolute Maximum Ratings[2]

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +6.5	V
Input Voltage (Referenced to GND)	V_{IN}	-0.5 to +6.5	V
Input Clamp Current	I_{IK}	-50	mA
Switch I/O Voltage (Referenced to GND)	V_{SW}	-0.5 to V_{CC} +0.5	V
On-State Switch Current	I_{SW}	±50	mA
Switch Clamping Current	I_{SK}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Power Dissipation in Still Air[3]	P_D	250	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **3.** Measured in plastic TSSOP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[4] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{CC}	1.65	5.5	V
Switch I/O Voltage		V_{SW}	0	5.5	V
High-Level Input Voltage, Enable Input	V_{CC} = 1.65V to 1.95V	V_{IH}	0.65xV_{CC}	-	V
	V_{CC} = 2.3V to 2.7V		0.7xV_{CC}	-	
	V_{CC} = 3V to 3.6V		0.7xV_{CC}	-	
	V_{CC} = 4.5V to 5.5V		0.7xV_{CC}	-	
Low-Level Input Voltage, Enable Input	V_{CC} = 1.65V to 1.95V	V_{IL}	-	0.35xV_{CC}	V
	V_{CC} = 2.3V to 2.7V		-	0.3xV_{CC}	
	V_{CC} = 3V to 3.6V		-	0.3xV_{CC}	
	V_{CC} = 4.5V to 5.5V		-	0.3xV_{CC}	
Enable Input Voltage		V_{IN}	0	5.5	V
Operating Temperature Range		T_J	-55	+125	°C
Input Transition Rise & Fall Rate	V_{CC} = 1.65V to 1.95V	Δt / ΔV	0	20	ns/V
	V_{CC} = 2.3V to 2.7V		0	20	
	V_{CC} = 3V to 3.6V		0	10	
	V_{CC} = 4.5V to 5.5V		0	10	

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[6]	
Maximum High-Level Input Voltage	V_{IH}	1.65 - 1.95V		$0.65xV_{CC}$	$0.65xV_{CC}$	$0.65xV_{CC}$	V
		2.3 - 2.7V		$0.7xV_{CC}$	$0.7xV_{CC}$	$0.7xV_{CC}$	
		2.7 - 3.6V		$0.7xV_{CC}$	$0.7xV_{CC}$	$0.7xV_{CC}$	
		4.5 - 5.5V		$0.7xV_{CC}$	$0.7xV_{CC}$	$0.7xV_{CC}$	
Maximum Low-Level Input Voltage	V_{IL}	1.65 - 1.95V		$0.35xV_{CC}$	$0.35xV_{CC}$	$0.35xV_{CC}$	V
		2.3 - 2.7V		$0.3xV_{CC}$	$0.3xV_{CC}$	$0.3xV_{CC}$	
		2.7 - 3.6V		$0.3xV_{CC}$	$0.3xV_{CC}$	$0.3xV_{CC}$	
		4.5 - 5.5V		$0.3xV_{CC}$	$0.3xV_{CC}$	$0.3xV_{CC}$	
On-State Switch Resistance[5]	r_{ON}	1.65V	$V_{IN}=V_{CC}$ or GND, I_{SW} = 4mA, OE = V_{IH}	12.5	30	45	Ω
		2.3V	$V_{IN}=V_{CC}$ or GND, I_{SW} = 8mA, OE = V_{IH}	9	20	30	
		3V	$V_{IN}=V_{CC}$ or GND, I_{SW} =24mA, OE = V_{IH}	7.5	15	23	
		4.5V	$V_{IN}=V_{CC}$ or GND, I_{SW} =32mA, OE = V_{IH}	6	10	15	
Peak On-State Resistance[5]	$r_{ON(P)}$	1.65V	$V_{IN}=V_{CC}$ to GND, I_{SW} = 4mA, OE = V_{IH}	85	130	195	Ω
		2.3V	$V_{IN}=V_{CC}$ to GND, I_{SW} = 8mA, OE = V_{IH}	22	30	45	
		3V	$V_{IN}=V_{CC}$ to GND, I_{SW} =24mA, OE = V_{IH}	12	20	30	
		4.5V	$V_{IN}=V_{CC}$ to GND, I_{SW} =32mA, OE = V_{IH}	7.5	15	23	
On-State Resistance difference between Switches	Δr_{ON}	1.65V	$V_{IN}=V_{CC}$ to GND, I_{SW} = 4mA, OE = V_{IH}	7	7	7	Ω
		2.3V	$V_{IN}=V_{CC}$ to GND, I_{SW} = 8mA, OE = V_{IH}	5	5	5	
		3V	$V_{IN}=V_{CC}$ to GND, I_{SW} =24mA, OE = V_{IH}	3	3	3	
		4.5V	$V_{IN}=V_{CC}$ to GND, I_{SW} =32mA, OE = V_{IH}	2	2	2	

5. 25°C values specified as Typical **6.** -55°C ≤ T_J ≤ +125°C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[6]	
Off-State Switch Leakage Current	$I_{SW(OFF)}$	5.5V	V_{IN} = V_{CC} V_{OUT} = GND, V_{IN} = GND V_{OUT} = V_{CC}, OE = V_{IL}	±0.1	±0.2	±1	µA
On-State Switch Leakage Current	$I_{SW(ON)}$	5.5V	V_{IN} = V_{CC} or GND, OE = V_{IH}, V_{OUT} = Open	±0.1	±1	±2	µA
Enable Input Current	I_{IN}	5.5V	OE = V_{CC} or GND,	±0.1	±1	±1	µA
Supply Current	I_{CC}	5.5V	V_{SW} = V_{CC} or GND	1	1	4	µA
Additional Supply Current	ΔI_{CC}	5.5V	One input at V_{CC} - 0.6V, other inputs GND or V_{CC}	500	500	500	µA
Enable Input Capacitance	C_{IN}	5V		TYPICAL			pF
				3.5			
Switch Input/Output Capacitance	$C_{IO(OFF)}$	5V		6			pF
	$C_{IO(ON)}$			14			
Power Dissipation Capacitance	C_{PD}	1.8V	f = 10MHz, T_A = 25°C	8			pF
		2.5V		9			
		3.3V		9.5			
		5V		11			

AC Electrical Characteristics[7]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Propagation Delay, Input A or B to Output B or A[8]	t_{PLH} / t_{PHL} (t_{pd})	1.8 ±0.15V	C_L = 30pF, R_L = 1kΩ	2	2	3	ns
		2.5 ±0.2V	C_L = 30pF, R_L = 500Ω	1.2	1.2	2	ns
		3.3 ±0.3V	C_L = 50pF, R_L = 500Ω	0.8	0.8	1.5	ns
		5 ±0.5V	C_L = 50pF, R_L = 500Ω	0.6	0.6	1	ns

7. Not production tested in die form, characterized by chip design and tested in package **8.** The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

AC Electrical Characteristics Continued[7]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Propagation Delay, Enable to Output A or B	t_{PZL} / t_{PZH} (t_{en})	1.8 ±0.15V	C_L = 30pF, R_L = 1kΩ,	10	10	13	ns
		2.5 ±0.2V	C_L = 30pF, R_L = 500Ω,	5.6	5.6	7.5	
		3.3 ±0.3V	C_L = 50pF, R_L = 500Ω,	4.4	4.4	6	
		5 ±0.5V	C_L = 50pF, R_L = 500Ω,	3.9	3.9	5	
Propagation Delay, Disable to Output A or B	t_{PLZ} / t_{PHZ} (t_{dis})	1.8 ±0.15V	C_L = 30pF, R_L = 1kΩ,	10.5	10.5	11.5	ns
		2.5 ±0.2V	C_L = 30pF, R_L = 500Ω,	6.9	6.9	8.5	
		3.3 ±0.3V	C_L = 50pF, R_L = 500Ω,	7.2	7.2	8	
		5 ±0.5V	C_L = 50pF, R_L = 500Ω,	6.3	6.3	6.5	

Analog Switching Characteristics[7] (T_A = 25°C)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				MIN	TYPICAL	MAX	
Frequency Response (Switch On), Input A or B to Output A or B	f_{MAX}	1.65V	C_L = 50pF, R_L = 600Ω, f_{IN} = sine wave	-	35	-	MHz
		2.3V		-	120	-	
		3V		-	175	-	
		4.5V		-	195	-	
		1.65V	C_L = 5pF, R_L = 50Ω, f_{IN} = sine wave	-	>300	-	
		2.3V		-	>300	-	
		3V		-	>300	-	
		4.5V		-	>300	-	
Crosstalk between Switches[8], Input A or B to Output A or B	V_{CT}	1.65V	C_L = 50pF, R_L = 600Ω, f_{IN} = 1MHz sine wave	-	-58	-	dB
		2.3V		-	-58	-	
		3V		-	-58	-	
		4.5V		-	-58	-	
		1.65V	C_L = 5pF, R_L = 50Ω, f_{IN} = 1MHz sine wave	-	-42	-	
		2.3V		-	-42	-	
		3V		-	-42	-	
		4.5V		-	-42	-	

8. Adjust f_{in} voltage to obtain 0 dBm at input

Analog Switching Characteristics continued[7] (T_A = 25°C)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				MIN	TYPICAL	MAX	
Crosstalk between Digital Inputs and Switch, OE to A or B	V_{CT}	1.65V	C_L = 50pF, R_L = 600Ω, f_{IN} = 1MHz square wave	-	35	-	dB
		2.3V		-	50	-	
		3V		-	70	-	
		4.5V		-	100	-	
Feed-through attenuation (Switch Off), Input A or B to Output A or B	$\alpha_{off(fT)}$	1.65V	C_L = 50pF, R_L = 600Ω, f_{IN} = 1MHz sine wave	-	-58	-	dB
		2.3V		-	-58	-	
		3V		-	-58	-	
		4.5V		-	-58	-	
		1.65V	C_L = 5pF, R_L = 50Ω, f_{IN} = 1MHz sine wave	-	-42	-	dB
		2.3V		-	-42	-	
		3V		-	-42	-	
		4.5V		-	-42	-	
Sine-Wave Distortion, Input A or B to Output A or B	THD	1.65V	C_L = 50pF, R_L = 10kΩ, f_{IN} = 1KHz sine wave	-	0.100	-	%
		2.3V		-	0.025	-	
		3V		-	0.015	-	
		4.5V		-	0.010	-	
		1.65V	C_L = 50pF, R_L = 10kΩ, f_{IN} = 10KHz sine wave	-	0.150	-	%
		2.3V		-	0.025	-	
		3V		-	0.015	-	
		4.5V		-	0.010	-	

Switching Waveforms

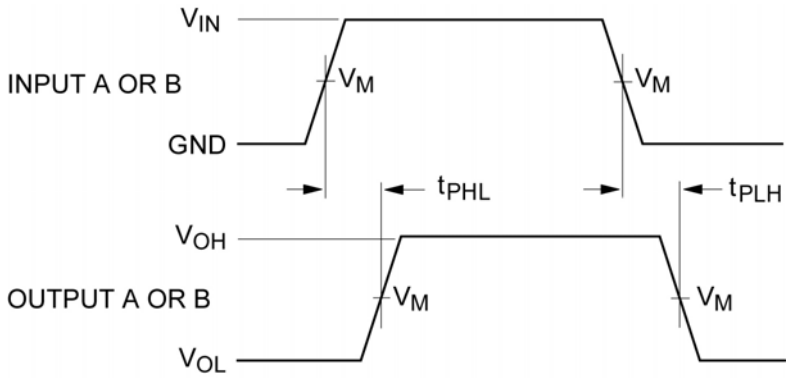


Figure 1 – Propagation Delay Input to Output

Switching Waveforms continued

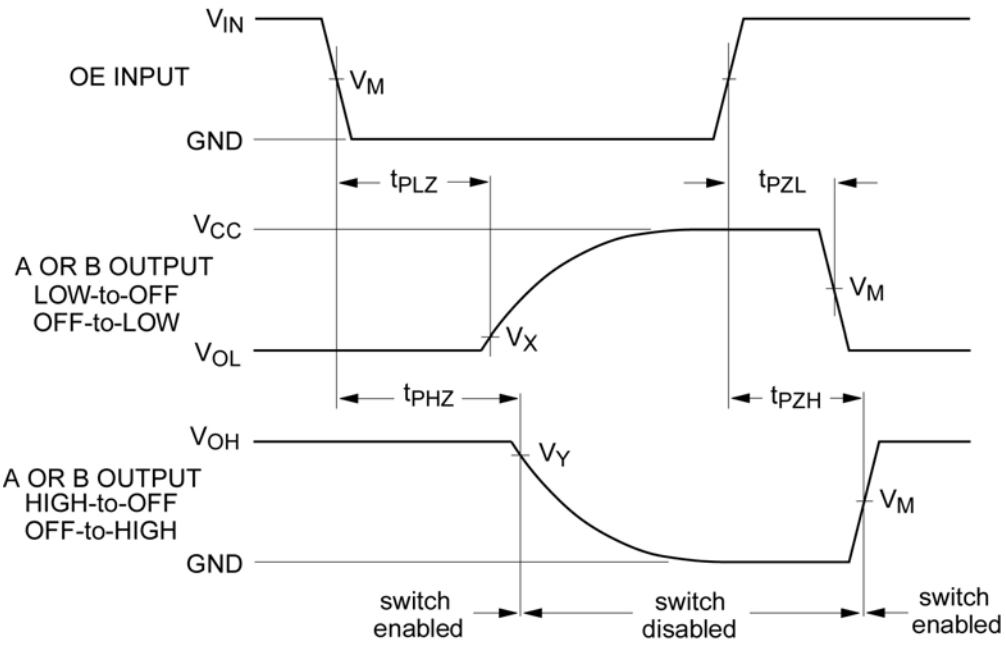
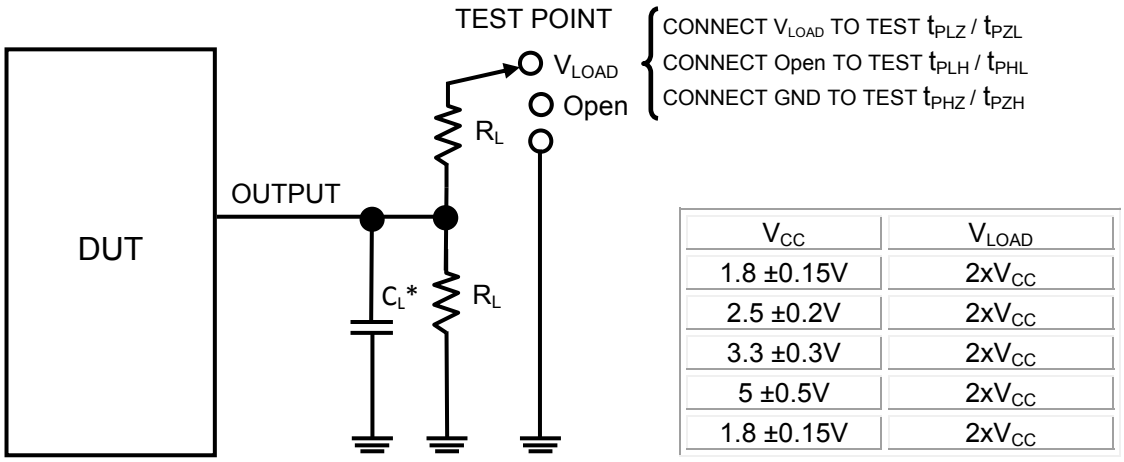


Figure 2 – Enable & Disable Timing, Switch

FIGURE 1 & 2 MEASUREMENT POINTS								
Supply	Input		V_M	V_{EXT}			V_X	V_Y
V_{CC}	V_{IN}	t_r / t_f		t_{PZL}, t_{PLZ}	t_{PZH}, t_{PHZ}	t_{PHL}, t_{PLH}		
1.8 ±0.15V	V_{CC}	≤2 ns	0.5xV_{CC}	2xV_{CC}	GND	open	V_{OL} +0.15V	V_{OH} -0.15V
2.5 ±0.2V	V_{CC}	≤2 ns	0.5xV_{CC}	2xV_{CC}	GND	open	V_{OL} +0.15V	V_{OH} -0.15V
3.3 ±0.3V	V_{CC}	≤2.5 ns	0.5xV_{CC}	2xV_{CC}	GND	open	V_{OL} +0.3V	V_{OH} -0.3V
5 ±0.5V	V_{CC}	≤2.5 ns	0.5xV_{CC}	2xV_{CC}	GND	open	V_{OL} +0.3V	V_{OH} -0.3V

Test Circuit



V_{CC}	V_{LOAD}
1.8 ±0.15V	$2xV_{CC}$
2.5 ±0.2V	$2xV_{CC}$
3.3 ±0.3V	$2xV_{CC}$
5 ±0.5V	$2xV_{CC}$
1.8 ±0.15V	$2xV_{CC}$

* Includes all probe and jig capacitance

Figure 3 – Test Setup