Low Voltage CMOS Logic – 54LVC1G125

Single Non-Inverting Buffer/Line Driver with 3-State Output in bare die form

Rev 1.0
29/06/19

Description

The 54LVC1G125 is a single non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input ($\overline{OE}$). A HIGH-level at pin $\overline{OE}$ sets the output to a high-impedance OFF-state. The device is driven by 3.3V or 5V inputs enabling use of this device in a mixed voltage environment. The part operates over a 1.65V to 5.5V supply range and is fully specified for partial power-down applications using I_{OFF}. I_{OFF} circuitry disables the output and prevents damaging backflow current through the device at power down. The device suits level translation and interfacing TTL to CMOS logic.

Features:

- Inputs directly interface TTL
- Inputs accept up to 5.5V enabling level translation down to V_{CC}
- Wide Supply Voltage: V_{CC} 1.65V - 5.5V
- Output Drive capability: ±24mA, V_{CC} = 3V
- Low Quiescent Current: 10µA max
- High speed: t_{pd} 6ns max, V_{CC} = 3V
- Full Military Temperature Range
- Tiny die size.

Ordering Information

The following part suffixes apply:

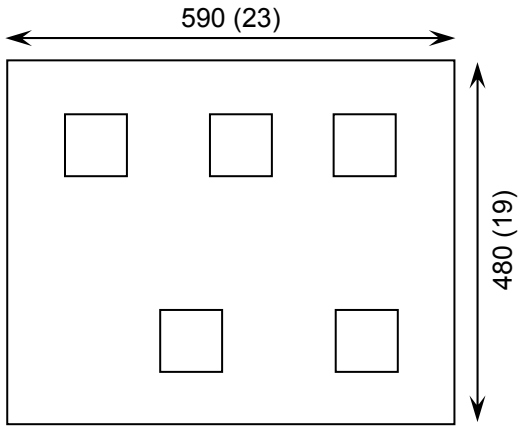
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	590 x 480 23 x 19	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±20) 11.02 (±0.79)	µm mils
Top Metal Composition	Al-Si-Cu 3 µm	
Back Metal Composition	N/A – Bare Si	

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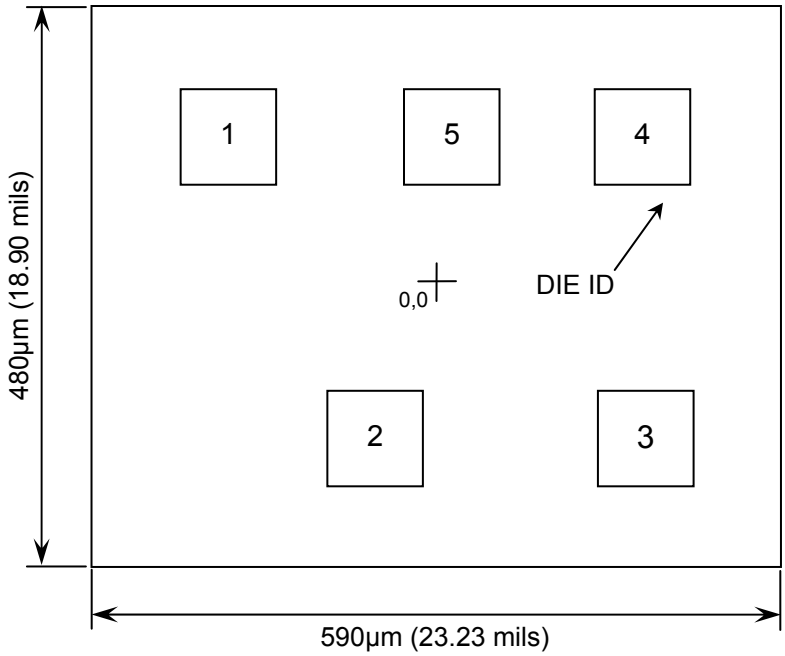
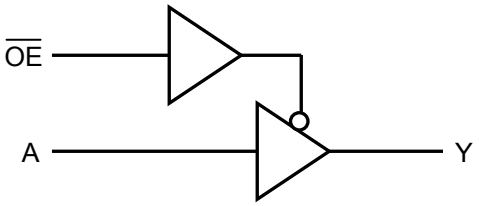
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	$\overline{OE}$	-178	130
2	V_{CC}	-51	-130
3	Y	180	-130
4	GND	178.1	130
5	A	14	130
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram

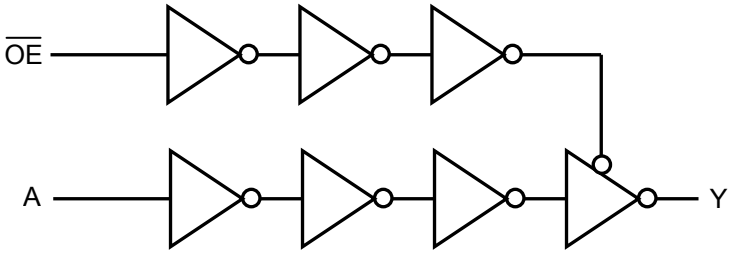


Truth Table

INPUTS		OUTPUT
A	$\overline{OE}$	Y
H	L	H
L	L	L
X	H	Z

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance
X = Don't care

Expanded Logic Diagram



Absolute Maximum Ratings[2]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +6.5	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to +6.5	V
DC Output Voltage – Active Mode	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Output Voltage – Power-Down, High Z, V_{CC}= 0V		-0.5 to +6.5	V
DC Input Clamp Current, $V_{IN} < 0$	I_{IK}	-50	mA
DC Output Clamp Current, $V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	I_{OK}	±50	mA
DC Output Current, V_{OUT} = 0V to V_{CC}	I_{OUT}	±50	mA
DC V_{CC} or GND Current	I_{CC}	±100	mA
Power Dissipation in Still Air[3]	P_D	250	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **3.** Measured in plastic TSSOP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[4] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	1.65	5.5	V
DC Supply Voltage – Data retention only		V_{CC}	1.5	-	V
DC Input Voltage		V_{IN}	0	5.5	V
DC Output Voltage		V_{OUT}	0	V_{CC}	V
High-Level Output Current	V_{CC} = 1.65V	I_{OH}	-	-4	mA
	V_{CC} = 2.3V		-	-8	
	V_{CC} = 2.7V		-	-12	
	V_{CC} = 3V		-	-24	
	V_{CC} = 4.5V		-	-32	
Low-Level Output Current	V_{CC} = 1.65V	I_{OL}	-	4	mA
	V_{CC} = 2.3V		-	8	
	V_{CC} = 2.7V		-	12	
	V_{CC} = 3V		-	24	
	V_{CC} = 4.5V		-	32	
Operating Temperature Range		T_J	-55	+125	°C
Input Transition Rise & Fall Rate	V_{CC} = 1.65V - 2.7V	Δt / ΔV	0	20	ns/V
	V_{CC} = 2.7V - 5.5V		0	10	ns/V

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum High-Level Input Voltage	V_{IH}	1.65 - 1.95V		0.65 x V_{CC}	0.65 x V_{CC}	0.65 x V_{CC}	V
		2.3 - 2.7V		1.7	1.7	1.7	
		2.7 - 3.6V		2.0	2.0	2.0	
		4.5 - 5.5V		0.7 x V_{CC}	0.7 x V_{CC}	0.7 x V_{CC}	
Maximum Low-Level Input Voltage	V_{IL}	1.65 - 1.95V		0.35 x V_{CC}	0.35 x V_{CC}	0.35 x V_{CC}	V
		2.3 - 2.7V		0.7	0.7	0.7	
		2.7 - 3.6V		0.8	0.8	0.8	
		4.5 - 5.5V		0.3 x V_{CC}	0.3 x V_{CC}	0.3 x V_{CC}	
Minimum High-Level Output Voltage	V_{OH}	1.65 - 5.5V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = -100µA	V_{CC} -0.1	V_{CC} -0.1	V_{CC} -0.1	V
		1.65V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = -4mA	1.2	1.2	0.95	
		2.3V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = -8mA	1.9	1.9	1.7	
		2.7V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = -12mA	2.2	2.2	1.9	V
		3.0V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = -24mA	2.3	2.3	2.0	
		4.5V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = -32mA	3.8	3.8	3.4	
Maximum Low-Level Output Voltage	V_{OL}	1.65 - 5.5V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 100µA	0.1	0.1	0.1	V
		1.65V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 4mA	0.45	0.45	0.70	
		2.3V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 8mA	0.3	0.3	0.45	
		2.7V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 12mA	0.4	0.4	0.60	V
		3.0V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 24mA	0.55	0.55	0.80	
		4.5V	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 32mA	0.55	0.55	0.80	
Input Leakage Current	I_{IN}	0V - 5.5V	V_{IN} = 5.5V or GND	±1	±1	±5	µA
OFF-State Output Current	I_{OZ}	3.6V	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 5.5V or GND	±2	±2	±10	µA

5. -55˚C ≤ T_J ≤ +125˚C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Power-Off Leakage Current	I_{OFF}	0V	V_{IN} or V_{OUT} = 5.5V	±2	±2	±10	µA
Supply Current	I_{CC}	1.65 -5.5V	V_{IN} = 5.5V or GND, I_{OUT} = 0A	4	4	10	µA
Additional Supply Current	ΔI_{CC}	2.3 - 5.5V	V_{IN} = V_{CC} - 0.6V, I_{OUT} =0A, Per pad	500	500	500	µA
Input Capacitance	C_{IN}	3.3V	V_{IN} = GND to V_{CC}, T_J = 25°C	TYPICAL			pF
				5			

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Propagation Delay Input A to Output Y (Figure 1,3)	t_{PLH} / t_{PHL}	1.65 - 1.95V	C_L = 30pF, Input t_r = t_f ≤ 2ns, R_L = 1kΩ, V_{IN} = V_{CC}	8	8	10.5	ns
		2.3 - 2.7V	C_L = 30pF, Input t_r = t_f ≤ 2ns, R_L = 500Ω, V_{IN} = V_{CC}	5.5	5.5	7.0	
		2.7V	C_L = 50pF, Input t_r = t_f ≤ 2.5ns, R_L = 500Ω, V_{IN} = 2.7V	5.5	5.5	7.0	
		3.0 - 3.6V	C_L = 50pF, Input t_r = t_f ≤ 2.5ns, R_L = 500Ω, V_{IN} = 2.7V	4.5	4.5	6.0	
		4.5 - 5.5V	C_L = 50pF, Input t_r = t_f ≤ 2.5ns, R_L = 500Ω, V_{IN} = V_{CC}	4.0	4.0	5.5	

6. Not production tested in die form, characterized by chip design and tested in package

AC Electrical Characteristics Continued[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Enable Time $\overline{OE}$ to Y (Figure 2,3)	t_{PZH} / t_{PZL}	1.65 - 1.95V	C_L = 30pF, Input $t_r = t_f \leq$ 2ns, R_L = 1kΩ, $V_{IN} = V_{CC}$	9.4	9.4	12	ns
		2.3 - 2.7V	C_L = 30pF, Input $t_r = t_f \leq$ 2ns, R_L = 500Ω, $V_{IN} = V_{CC}$	6.6	6.6	8.5	
		2.7V	C_L = 50pF, Input $t_r = t_f \leq$ 2.5ns, R_L = 500Ω, V_{IN} = 2.7V	6.6	6.6	8.5	
		3.0 - 3.6V	C_L = 50pF, Input $t_r = t_f \leq$ 2.5ns, R_L = 500Ω, V_{IN} = 2.7V	5.3	5.3	7	
		4.5 - 5.5V	C_L = 50pF, Input $t_r = t_f \leq$ 2.5ns, R_L = 500Ω, $V_{IN} = V_{CC}$	5.0	5.0	6.5	
Disable Time $\overline{OE}$ to Y (Figure 2,3)	t_{PLZ} / t_{PHZ}	1.65 - 1.95V	C_L = 30pF, Input $t_r = t_f \leq$ 2ns, R_L = 1kΩ, $V_{IN} = V_{CC}$	9.2	9.2	12	ns
		2.3 - 2.7V	C_L = 30pF, Input $t_r = t_f \leq$ 2ns, R_L = 500Ω, $V_{IN} = V_{CC}$	5.0	5.0	6.5	
		2.7V	C_L = 50pF, Input $t_r = t_f \leq$ 2.5ns, R_L = 500Ω, V_{IN} = 2.7V	5.0	5.0	6.5	
		3.0 - 3.6V	C_L = 50pF, Input $t_r = t_f \leq$ 2.5ns, R_L = 500Ω, V_{IN} = 2.7V	5.0	5.0	6.5	
		4.5 - 5.5V	C_L = 50pF, Input $t_r = t_f \leq$ 2.5ns, R_L = 500Ω, $V_{IN} = V_{CC}$	4.2	4.2	5.5	
Power Dissipation Capacitance[7]	C_{PD}	-	V_{IN} = GND to V_{CC}, T_J = 25°C	TYPICAL			pF
				Output Enabled		25	
				Output Disabled		6	

6. Not production tested in die form, characterized by chip design and tested in package. **7.** Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ in microwatts.

Switching Waveforms

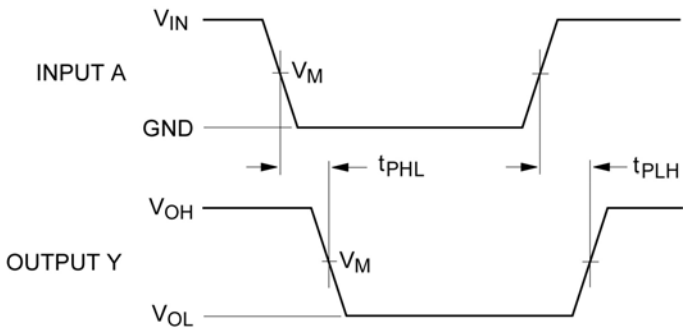


Figure 1 – Propagation Delay Input to Output

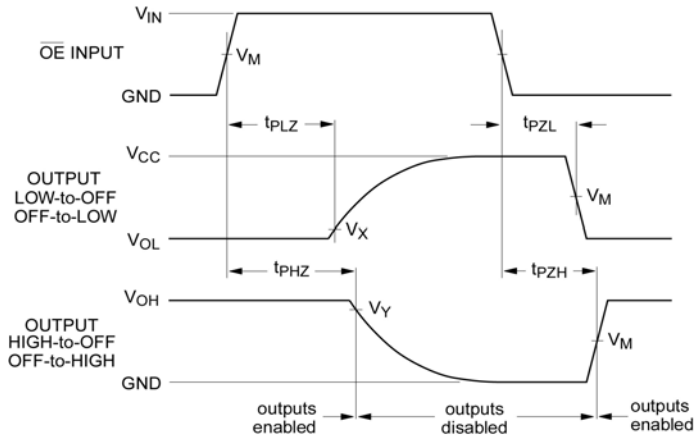
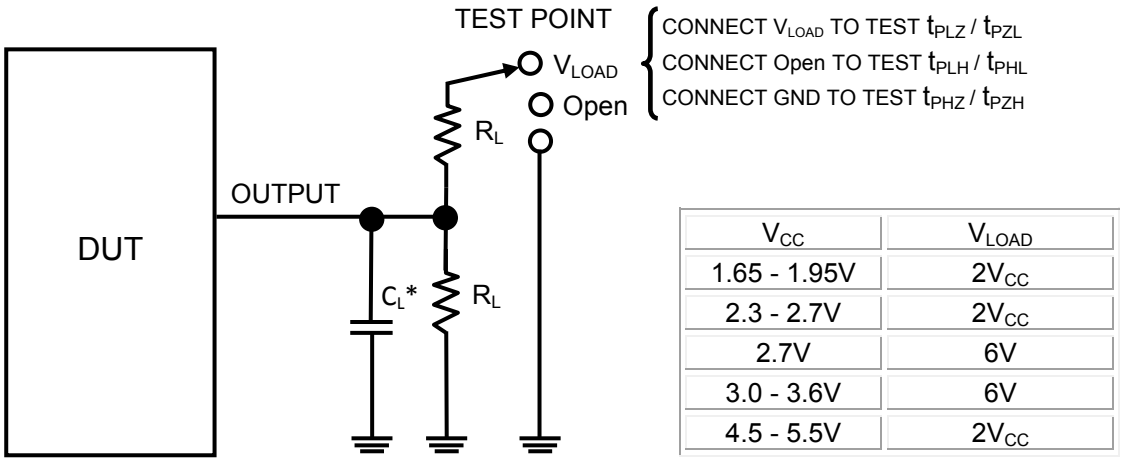


Figure 2 – Enable & Disable Timing, 3-State

MEASUREMENT POINTS					
V_{CC}	V_{IN}	V_M (INPUT)	V_M (OUTPUT)	V_X	V_Y
1.65 - 1.95V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} +0.15V	V_{OH} -0.15V
2.3 - 2.7V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} +0.15V	V_{OH} -0.15V
2.7V	2.7V	1.5V	1.5V	V_{OL} +0.3V	V_{OH} -0.3V
3.0 - 3.6V	2.7V	1.5V	1.5V	V_{OL} +0.3V	V_{OH} -0.3V
4.5 - 5.5V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	0 V_{OL} +0.3V	V_{OH} -0.3V

Test Circuit



V_{CC}	V_{LOAD}
1.65 - 1.95V	$2V_{CC}$
2.3 - 2.7V	$2V_{CC}$
2.7V	6V
3.0 - 3.6V	6V
4.5 - 5.5V	$2V_{CC}$

* Includes all probe and jig capacitance

Figure 3 – Test Setup