Low Power Schottky Logic – 54LS86A

Quadruple 2-Input Exclusive OR Gate IC in bare die form

Rev 1.0
21/11/17

Description

The 54LS86A is fabricated using a 2µm 40V Bipolar process. The device contains four independent gates and performs the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic. The device is characterized over the full Military Temperature Range.

Features:

- High speed – 22ns (Typ) propagation delay
- Low Power – I_{CC} 10mA Max
- Full Military Temperature Range.
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

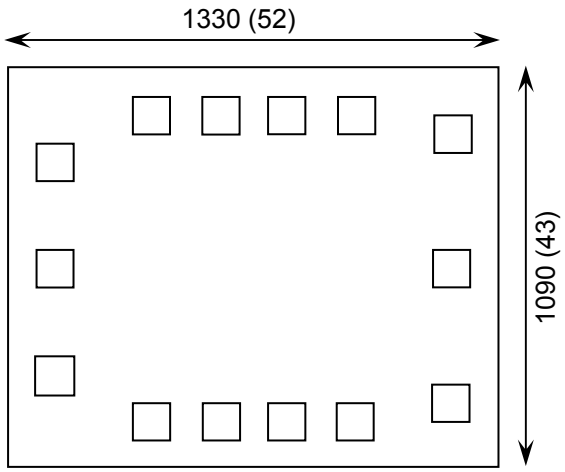
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1330 x 1090 52 x 43	µm mils
Minimum Bond Pad Size	98 x 98 3.86 x 3.86	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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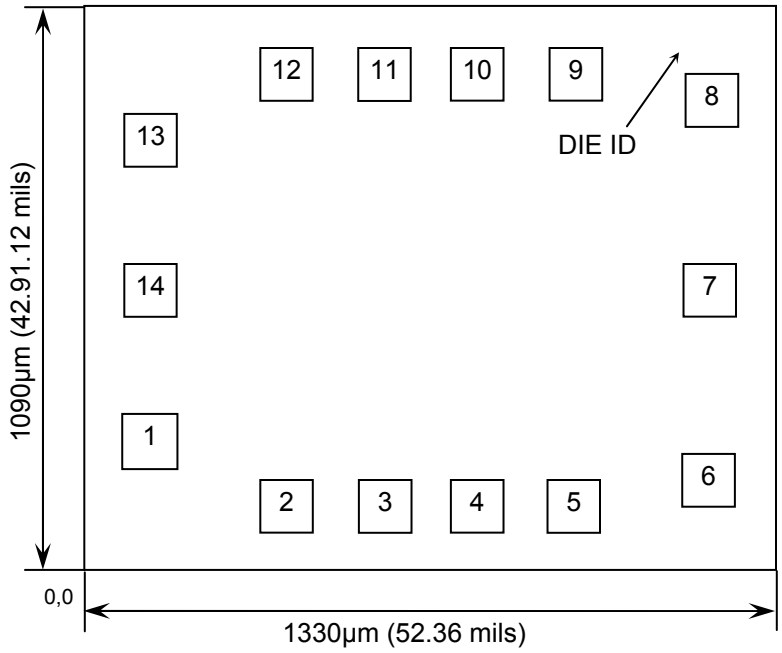
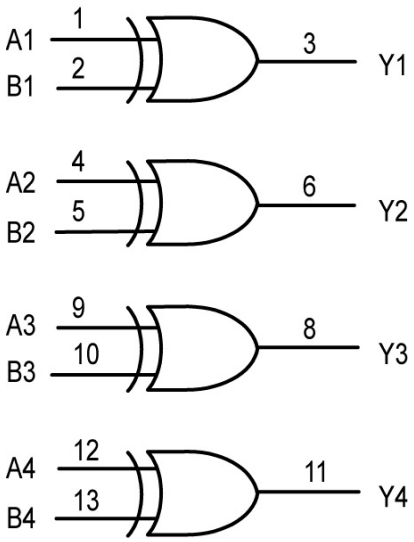
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A1	0.077	0.205
2	B1	0.338	0.079
3	Y1	0.528	0.079
4	A2	0.704	0.079
5	B2	0.894	0.079
6	Y2	1.154	0.129
7	GND	1.154	0.496
8	Y3	1.154	0.863
9	A3	0.894	0.913
10	B3	0.704	0.913
11	Y4	0.528	0.913
12	A4	0.338	0.913
13	B4	0.077	0.787
14	V_{CC}	0.077	0.496
CONNECT CHIP BACK TO GND OR FLOAT			

Logic Diagram



$Y = A \oplus B$
$= \overline{A}B + A\overline{B}$

Pad 14 = V_{CC}
Pad 7 = GND

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High level (steady state)
L = Low level (steady state)

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{CC}	7.0	V
DC Input Voltage	V_{IN}	7.0	V
DC Input Voltage	V_{OUT}	5.5	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.7	V
High-Level Output Current	I_{OH}	-	-0.4	mA
Low-Level Output Current	I_{OL}	-	4	mA
Operating Temperature Range	T_J	-55	+125	°C

DC Electrical Characteristics[2] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-		2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-		-	-	0.7	V
Input Clamp Diode Voltage	V_{IK}	V_{CC} = MIN I_{IN} = -18mA		-	-0.65	-1.5	V
Output Voltage High	V_{OH}	V_{CC} = MIN, I_{OH} = MAX V_{IN} = V_{IL} or V_{IH} per Function Table		2.5	3.4	-	V
Output Voltage Low	V_{OL}	V_{CC} = MIN I_{OH} = MAX V_{IN} = V_{IL} or V_{IH} per Truth Table	I_{OL} = 4mA	-	0.25	0.4	V
Input High Current	I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V		-	-	40	µA
		V_{CC} = MAX, V_{IN} = 7.0V		-	-	0.2	mA
Input Low Current	I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V		-	-	-0.8	mA
Short Circuit Current[3]	I_{OS}	V_{CC} = MAX		-20	-	-100	mA
Power Supply Current (Total)	I_{CC}	V_{CC} = MAX		-	6.1	10	mA

2. All typical values @ V_{CC} = 5V, T_J = 25°C. **3.** Not more than one output should be shorted at a time, nor for more than 1 second.

AC Electrical Characteristics[4]

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay, Other Input Low	t_{PLH}	V_{CC} = 5V, C_L = 15pF	-	12	23	ns
	t_{PHL}			10	17	
Propagation Delay, Other Input High	t_{PLH}	V_{CC} = 5V, C_L = 15pF	-	20	30	ns
	t_{PHL}		-	13	22	

4. Not production tested in die form, characterized by chip design and tested in package.