High Speed CMOS TTL Input – 54HCT373

8-bit transparent D-Type Latch with 3-State Outputs in bare die form

Rev 1.0
07/02/19

Description

The 54HCT373 consists of eight D-type transparent latches fabricated using a 2.5µm 5V CMOS process to combine high speed performance LSTTL performance with CMOS low power consumption. Each latch is equipped with separate D-Type inputs and 3-State outputs for bus oriented applications. Data output changes asynchronously and data may be latched even when the outputs are not enabled. Device inputs directly accept both standard CMOS and LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- TTL / CMOS compatible Input Levels
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- Function compatible with 54LS373
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

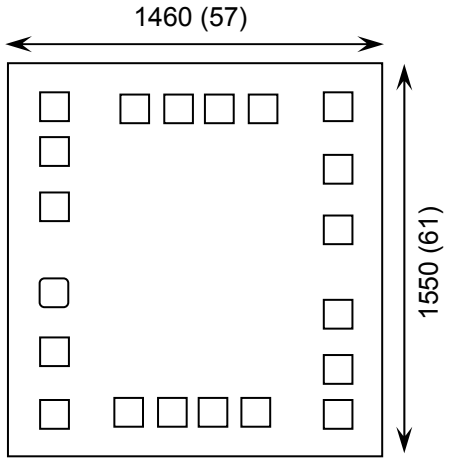
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1460 x 1550 57 x 61	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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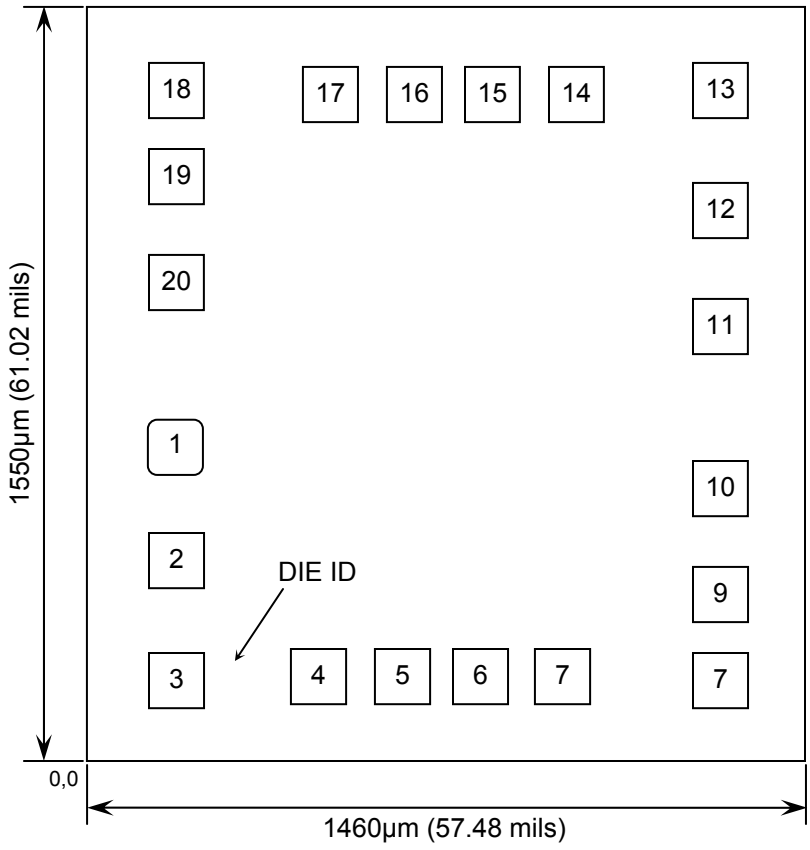
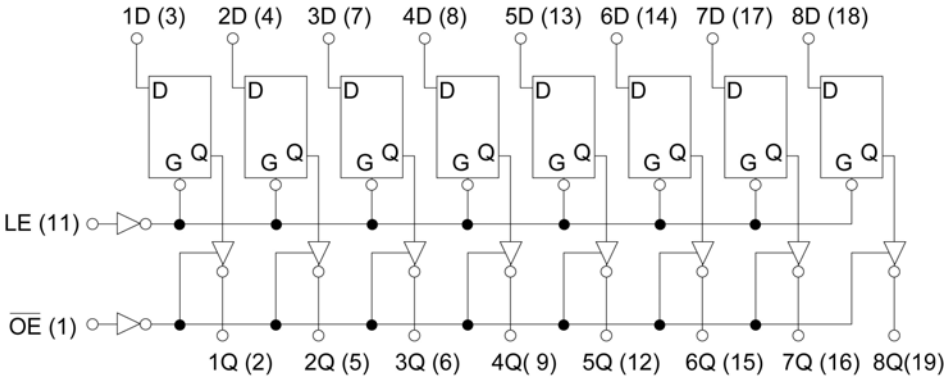
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{OE}$	0.1205	0.597
2	1Q	0.1205	0.3595
3	1D	0.1205	0.122
4	2D	0.413	0.1225
5	2Q	0.582	0.1225
6	3Q	0.7415	0.1225
7	3D	0.913	0.1225
8	4D	1.234	0.116
9	4Q	1.232	0.29
10	GND	1.232	0.51
11	LE	1.232	0.842
12	5Q	1.232	1.0795
13	5D	1.232	1.317
14	6D	0.9395	1.3165
15	6Q	0.7705	1.3165
16	7Q	0.611	1.3165
17	7D	0.4395	1.3165
18	8D	0.1185	1.323
19	8Q	0.1205	1.149
20	V_{CC}	0.1205	0.929
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 10 = GND, Pad 20 = V_{CC}

Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance
X = Don't care

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±35	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±75	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_J	-55	+125	°C
Input Rise or Fall Times	t_r, t_f	-	500	ns

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\|$ ≤ 20μA	2.0	2.0	2.0	V
		5.5V		2.0	2.0	2.0	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\|$ ≤ 20μA	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20μA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0mA	3.98	3.84	3.70	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20μA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0mA	0.26	0.33	0.40	

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State Leakage Current	I_{OZ}	5.5V	High Z Output, $V_{IN} = V_{IL}$ or V_{IH}, $V_{OUT}=V_{CC}$ or GND	±0.5	±5	±10	µA
Maximum Quiescent Supply Leakage Current[5]	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND $\lvert I_{OUT} \rvert \leq 0\mu A$	4	40	160	µA
Additional Quiescent Supply Current[5]	ΔI_{CC}	5.5V	V_{IN} = 2.4V, Any One Input. $V_{IN} = V_{CC}$ or GND, Other Inputs I_{OUT} = 0µA	**≥ -55°C**	**25°C to 125°C**		mA
				2.9	2.4		

4. -55°C ≤ T_J ≤ +125°C **5.** Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, D to Q (Figure 1,5)	t_{PLH}, t_{PHL}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	28	35	42	ns
Maximum Propagation Delay, LE to Q (Figure 2,5)	t_{PLH}, t_{PHL}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	32	40	48	ns
Maximum Propagation Delay, $\overline{OE}$ to Q (Figure 3,6)	t_{PLZ}, t_{PHZ}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	30	38	45	ns
Maximum Propagation Delay, $\overline{OE}$ to Q (Figure 3,6)	t_{PZL}, t_{PZH}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	35	44	53	ns
Maximum Output Transition Time, Any Output (Figure 1,5)	t_{TLH}, t_{THL}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	12	15	18	pF

6. Not production tested in die form, characterized by chip design and tested in package.

AC Electrical Characteristics continued[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Capacitance	C_{IN}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	10	10	10	pF
Maximum 3-State Output Capacitance	C_{OUT}	5V ±10%	C_L = 50pF, Input $t_r = t_f$ = 6ns	15	15	15	pF
Power Dissipation Capacitance per Latch[7]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				65			

6. Not production tested in die form, characterized by chip design and tested in package.
7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to LE (Figure 4)	t_{SU}	5V ±10%	Input $t_r = t_f$ =6ns	10	13	15	ns
Minimum Hold Time, LE to D (Figure 4)	t_h	5V ±10%	Input $t_r = t_f$ =6ns	10	13	15	ns
Minimum Pulse Width, LE (Figure 4)	t_w	5V ±10%	Input $t_r = t_f$ =6ns	12	15	18	ns
Maximum Input Rise & Fall Times (Figure 4)	t_r, t_f	5V ±10%	Input $t_r = t_f$ =6ns	500	500	500	ns

Switching Waveforms

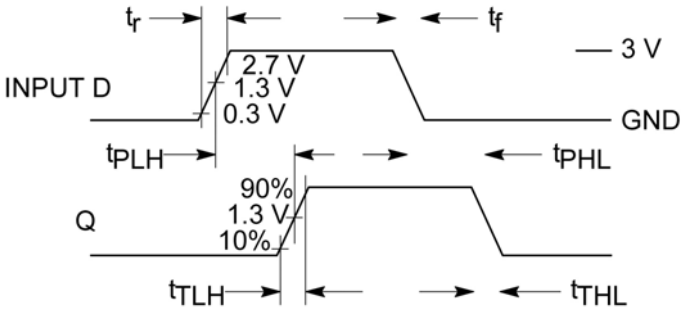


Figure 1 – Propagation Delay & Output Transition Time

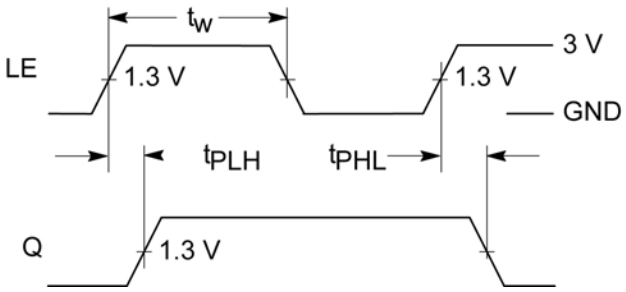


Figure 2 – Propagation Delay – Latch Enable to Q

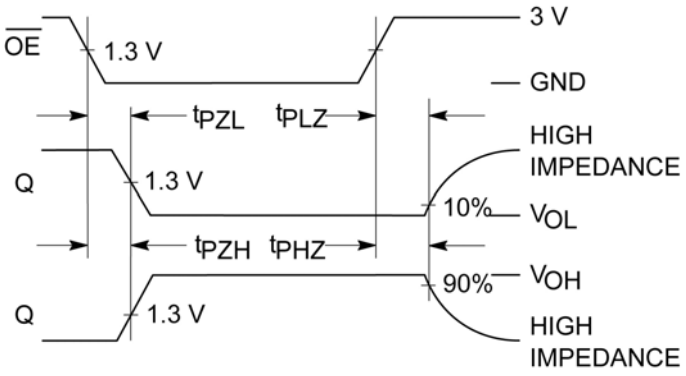


Figure 3 – Propagation Delay - Output Enable to Q

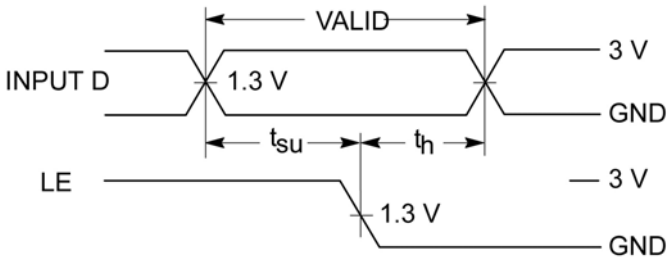
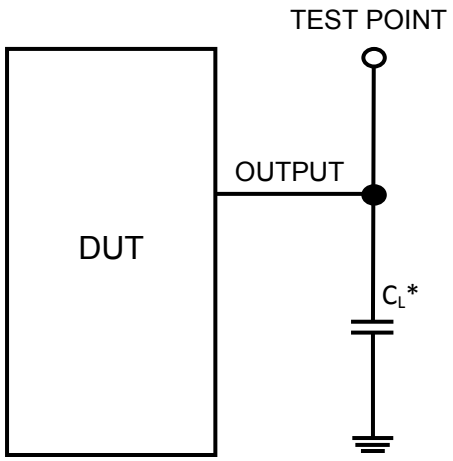


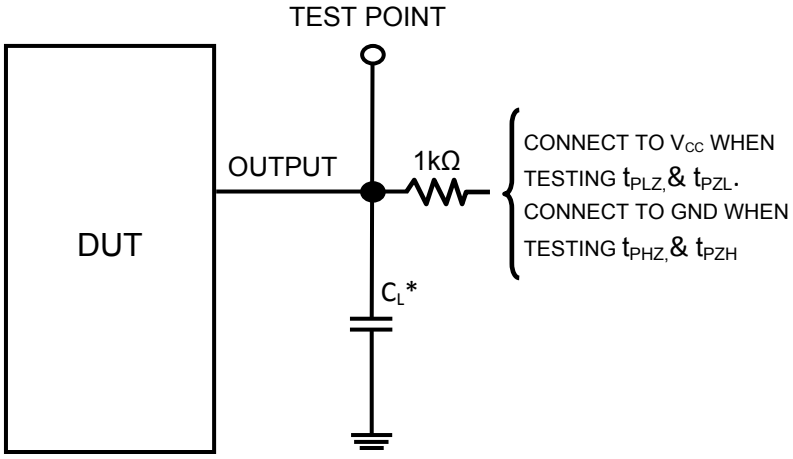
Figure 4 – Timing Requirements

Test Circuits



* Includes all probe and jig capacitance

Figure 5



* Includes all probe and jig capacitance

Figure 6