High Speed CMOS TTL Input – 54HCT04

Hex Inverter Logic IC with LSTTL compatible inputs in bare die form

Rev 1.0
24/11/17

Description

The 54HCT04 Hex Inverter is fabricated using a 2.5µm 5V CMOS process with the same high speed performance of LSTTL combined with CMOS low power consumption. The device is commonly used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs and contains six independent inverters with standard push-pull outputs which perform the Boolean function Y = Ā in positive logic. All inputs are protected against ESD and excess voltage transients. Device inputs directly accept LSTTL or CMOS.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- TTL / CMOS compatible Input Levels
- Function compatible with 54LS04
- Full Military Temperature range.

Ordering Information

The following part suffixes apply:

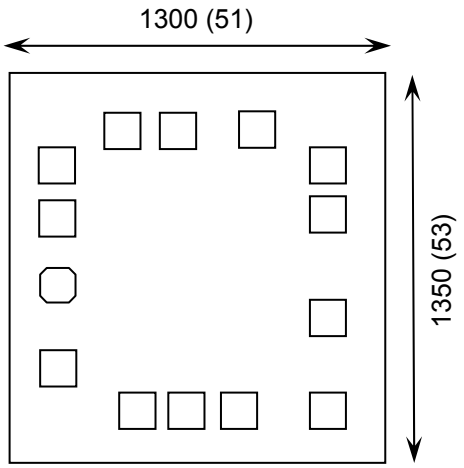
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1300 x 1350 51 x 53	µm mils
Minimum Bond Pad Size	100 x 100 4 x 4	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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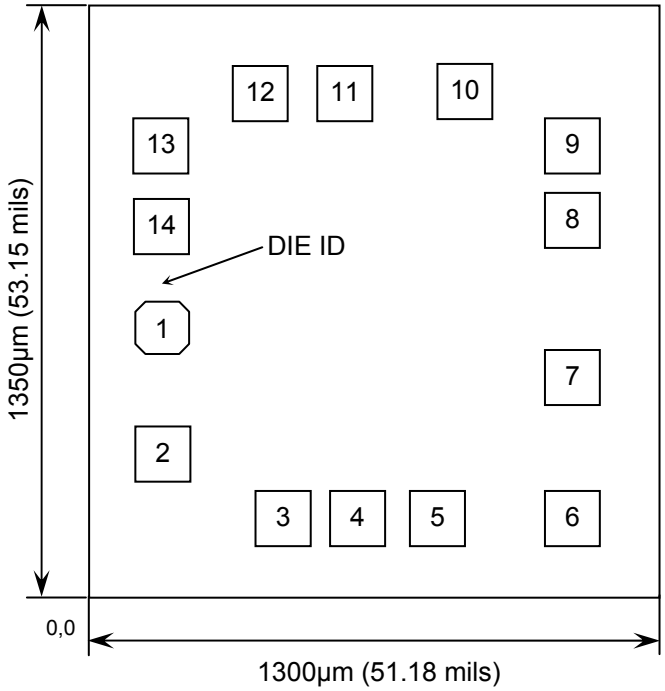
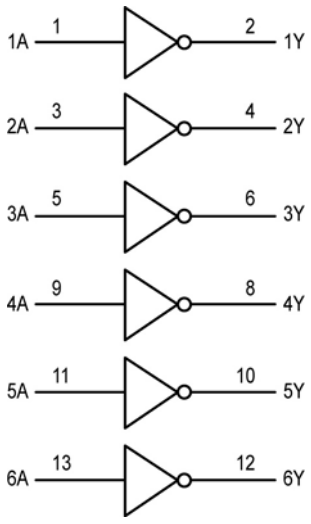
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.112	0.555
2	1Y	0.112	0.2705
3	2A	0.3815	0.120
4	2Y	0.5535	0.120
5	3A	0.7365	0.120
6	3Y	1.047	0.120
7	GND	1.047	0.4445
8	4Y	1.047	0.798
9	4A	1.047	0.967
10	Y5	0.802	1.085
11	5A	0.5295	1.085
12	6Y	0.338	1.085
13	6A	0.112	0.967
14	V_{CC}	0.112	0.7835
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



$Y = \bar{A}$

Pad 14 = V_{CC}
Pad 7 = GND

Function Table

INPUTS A	OUTPUT Y
H	L
L	H
H = High level (steady state)	
L = Low level (steady state)	

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_J	-55	+125	°C
Input Rise or Fall Times	t_r, t_f	-	500	ns

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	2.0	2.0	2.0	V
		5.5V		2.0	2.0	2.0	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	V_{IN} = V_{IL} $\lvert I_{OUT} \rvert$ ≤ 20µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IL} $\lvert I_{OUT} \rvert$ ≤ 4.0mA	3.98	3.84	3.70	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	V_{IN} = V_{IH} $\lvert I_{OUT} \rvert$ ≤ 20µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IH} $\lvert I_{OUT} \rvert$ ≤ 4.0mA	0.26	0.33	0.40	

4. -55˚C ≤ T_J ≤ +125˚C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current[3]	I_{CC}	5.5V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	1	10	40	µA
Additional Quiescent Supply Current[5]	ΔI_{CC}	5.5V	V_{IN} = 2.4V, Any One Input. V_{IN} = V_{CC} or GND, Other Inputs I_{OUT} = 0µA	**≥ -55°C**	**25°C to 125°C**		mA
				2.9	2.4		

5. Total Supply Current = I_{CC} + $\Sigma\Delta I_{CC}$.

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t_{PLH}	5V ±10%	C_L = 50pF, t_r = t_f = 6ns	15	19	22	ns
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t_{PHL}	5V ±10%	C_L = 50pF, t_r = t_f = 6ns	17	21	26	
Maximum Output Rise and Fall Time (Figure 1,2)	t_{TLH}, t_{THL}	5V ±10%	C_L = 50pF, t_r = t_f = 6ns	15	19	22	ns
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[7]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	**TYPICAL**			pF
				22			

6. Not production tested in die form, characterized by chip design and tested in package.
7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

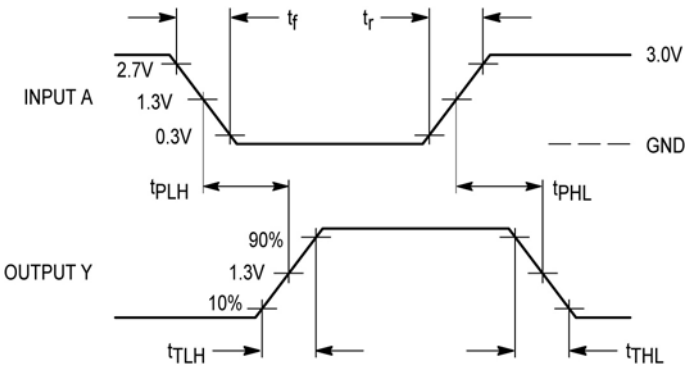
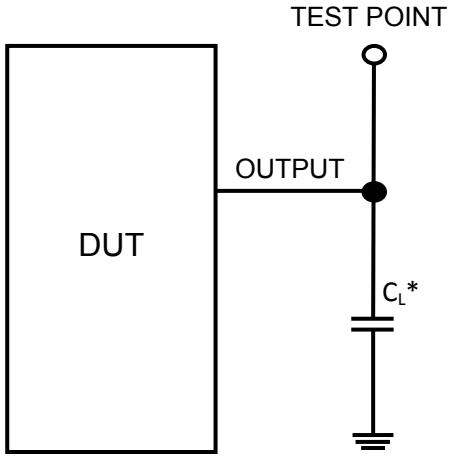


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



* Includes all probe and jig capacitance

Figure 2