



# High Speed CMOS Logic – 54HC595

8-bit shift registers with 3-state output latches in bare die form

Rev 1.2  
22/12/21

## Description

The 54HC595 is an 8-bit serial-in to parallel-out shift register which drives an 8-bit D-type latch with 3-state outputs. Both register and latch have independent positive triggered clock inputs. All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together the input shift register is always one clock cycle ahead of the output register. The shift register also features asynchronous reset. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

## Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS595
- Full Military Temperature Range.

## Ordering Information

The following part suffixes apply:

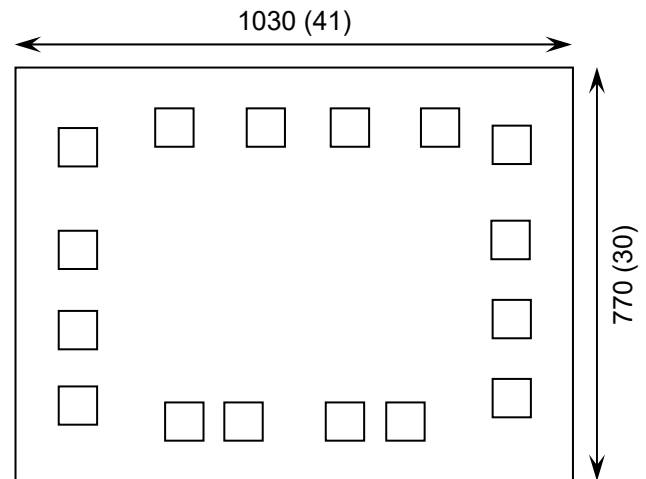
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

## Die Dimensions in µm (mils)



## Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1030 x 770 41 x 30	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±10) 11.02 (±0.39)	µm mils
Top Metal Composition	Al-Si-Cu 2.8 µm	
Back Metal Composition	N/A – Bare Si	

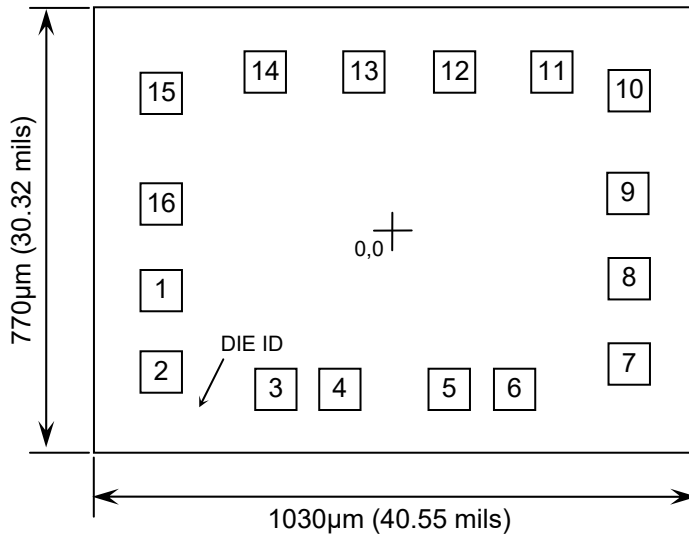




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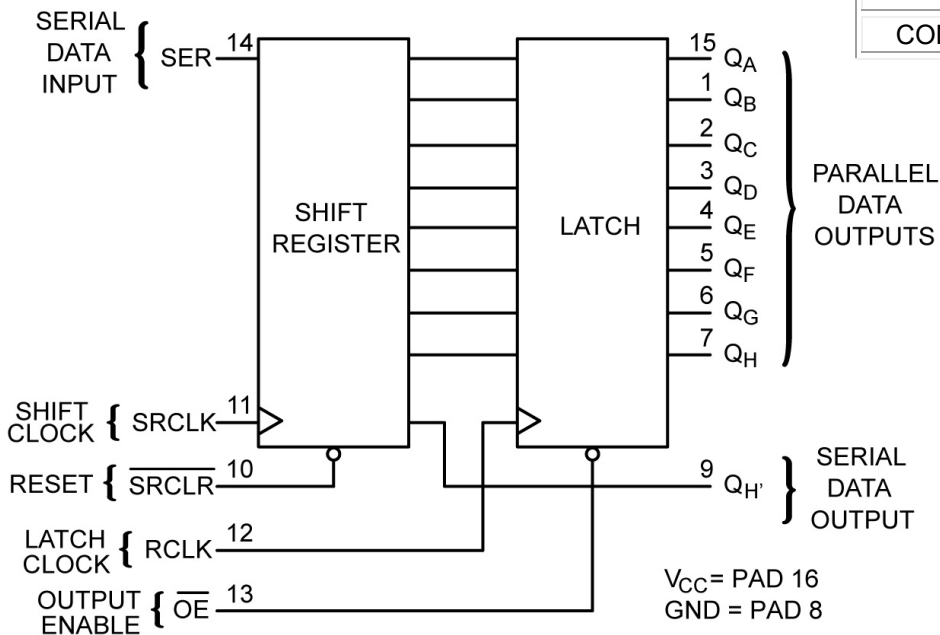
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	Q <sub>B</sub>	-401.8	-102
2	Q <sub>C</sub>	-401.8	-246
3	Q <sub>D</sub>	-205.8	-273
4	Q <sub>E</sub>	-95.8	-273
5	Q <sub>F</sub>	95.8	-273
6	Q <sub>G</sub>	205.8	-273
7	Q <sub>H</sub>	401.8	-230.2
8	GND	401.8	-84.6
9	Q <sub>H'</sub>	401.8	62.6
10	$\overline{\text{SRCLR}}$	401.8	243.2
11	SRCLK	272	273
12	RCLK	103.2	273
13	$\overline{\text{OE}}$	-54.4	273
14	SER	-233.2	273
15	Q <sub>A</sub>	-401.8	237.6
16	V <sub>CC</sub>	-401.8	46

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

## Logic Diagram





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## Function Table<sup>1</sup>

INPUTS					OUTPUTS		FUNCTION
SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	$Q_H'$	$Q_N$	
X	X	L	L	X	L	NC	LOW level on $\overline{SRCLR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift-register loaded into storage register
X	X	H	L	X	L	Z	Shift-register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	$Q_G'$	NC	Logic high level shifted into shift register stage 0. Content of all shift register stages shifted through, e.g. previous state of stage 6 (internal $Q_6'$ ) appears on serial output( $Q_H'$ )
X	↑	L	H	X	NC	$Q_n'$	Contents of shift register stages (internal $Q_n'$ ) transfers to the storage register and parallel output stages
↑	↑	L	H	X	$Q_G'$	$Q_n'$	Shift register contents shifted through. Previous shift register content transfers to storage register & parallel output stages.

1. H=HIGH voltage level; L=LOW voltage level; ↑=LOW-to-HIGH transition; Z=high-impedance OFF-state; NC=no change; X=don't care.

## Absolute Maximum Ratings<sup>2</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current, per pad	$I_{IN}$	±20	mA
DC Output Current, per pad	$I_{OUT}$	±35	mA
DC $V_{CC}$ or GND Current	$I_{CC}$	±75	mA
Power Dissipation in Still Air <sup>3</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 3. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>4</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	$V_{CC}$	2	6	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	-55	+125	°C	
Input Rise or Fall Times	$V_{CC} = 2.0V$	$t_r, t_f$	0	1000	ns
	$V_{CC} = 4.5V$		0	500	ns
	$V_{CC} = 6.0V$		0	400	ns

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.





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## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS	
				25°C	85°C	FULL RANGE <sup>5</sup>		
Minimum High-Level Input Voltage	V <sub>IH</sub>	2.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>OUT</sub>   ≤ 20μA	1.5	1.5	1.5	V	
		3.0V		2.1	2.1	2.1		
		4.5V		3.15	3.15	3.15		
		6.0V		4.2	4.2	4.2		
Maximum Low-Level Input Voltage	V <sub>IL</sub>	2.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>OUT</sub>   ≤ 20μA	0.5	0.5	0.5	V	
		3.0V		0.9	0.9	0.9		
		4.5V		1.35	1.35	1.35		
		6.0V		1.8	1.8	1.8		
Minimum High-Level Output Voltage (Q <sub>A</sub> – Q <sub>H</sub> )	V <sub>OH</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	1.9	1.9	1.9	V	
		4.5V		4.4	4.4	4.4		
		6.0V		5.9	5.9	5.9		
	V <sub>OH</sub>	3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 2.4mA	2.48	2.34	2.2	V	
		4.5V		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0mA	3.98	3.84		3.70
		6.0V			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 7.8mA	5.48		5.34
Maximum Low-Level Output Voltage (Q <sub>A</sub> – Q <sub>H</sub> )	V <sub>OL</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	0.1		0.1	0.1	V
		4.5V		0.1	0.1	0.1		
		6.0V		0.1	0.1	0.1		
	V <sub>OL</sub>	3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 2.4mA	0.26	0.33	0.40	V	
		4.5V		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0mA	0.26	0.33		0.40
		6.0V			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 7.8mA	0.26		0.33
Minimum High-Level Output Voltage (Q <sub>H</sub> )	V <sub>OH</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	1.9		1.9	1.9	V
		4.5V		4.4	4.4	4.4		
		6.0V		5.9	5.9	5.9		
	V <sub>OH</sub>	3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 2.4mA	2.48	2.34	2.20	V	
		4.5V		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0mA	3.98	3.84		3.70
		6.0V			V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 5.2mA	5.48		5.34

5. -55°C ≤ T<sub>J</sub> ≤ +125°C





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## DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>5</sup>	
Maximum Low-Level Output Voltage (Q <sub>H</sub> )	V <sub>OL</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 2.4mA	0.26	0.33	0.40	V
		4.5V		0.26	0.33	0.40	
		6.0V		V <sub>IN</sub> = V <sub>CC</sub> or GND  I <sub>OUT</sub>   ≤ 5.2mA	0.26	0.33	
Maximum Input Leakage Current	I <sub>IN</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Maximum Three-State Leakage Current (Q <sub>A</sub> –Q <sub>H</sub> )	I <sub>OZ</sub>	6.0V	High-Impedance Output State, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = V <sub>CC</sub> or GND	±0.5	±5.0	±10	μA
Maximum Quiescent Supply Current	I <sub>CC</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0μA	4	40	160	μA

## AC Electrical Characteristics<sup>6</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>5</sup>	
Maximum Clock Frequency (50% Duty Cycle) (Figure 1,7)	f <sub>max</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	6.0	4.8	4.0	MHz
		3.0V		15	10	8	
		4.5V		30	24	20	
		6.0V		35	28	24	
Maximum Propagation Delay, SRCLK to Q <sub>H</sub> (Figure 1,7)	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	140	175	210	ns
		3.0V		100	125	150	
		4.5V		28	35	42	
		6.0V		24	30	36	
Maximum Propagation Delay, SRCLR to Q <sub>H</sub> (Figure 2,7)	t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	145	180	220	ns
		3.0V		100	125	150	
		4.5V		29	36	44	
		6.0V		25	31	38	
Maximum Propagation Delay, RCLK to Q <sub>A</sub> – Q <sub>H</sub> (Figure 3,7)	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	140	175	210	ns
		3.0V		100	125	150	
		4.5V		28	35	42	
		6.0V		24	30	36	

6. Not production tested in die form, characterized by chip design and tested in package.





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## AC Electrical Characteristics continued<sup>6</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>5</sup>	
Maximum Propagation Delay, OE to Q <sub>A</sub> – Q <sub>H</sub> (Figure 4,8)	t <sub>PLZ</sub> , t <sub>PHZ</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	150	190	225	ns
		3.0V		100	125	150	
		4.5V		30	38	45	
		6.0V		26	33	38	
Maximum Propagation Delay, OE to Q <sub>A</sub> – Q <sub>H</sub> (Figure 4,8)	t <sub>PZL</sub> , t <sub>PZH</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	135	170	205	ns
		3.0V		90	110	130	
		4.5V		27	34	41	
		6.0V		23	29	35	
Maximum Output Transition Time, Q <sub>A</sub> – Q <sub>H</sub> (Figure 3,7)	t <sub>TLH</sub> , t <sub>THL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	60	75	90	ns
		3.0V		23	27	31	
		4.5V		12	15	18	
		6.0V		10	13	15	
Maximum Output Transition Time, Q <sub>H</sub> ' (Figure 1,7)	t <sub>TLH</sub> , t <sub>THL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	75	95	110	ns
		3.0V		27	32	36	
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	C <sub>IN</sub>	-	-	10	10	10	pF
Maximum Three-State Output Capacitance, Q <sub>A</sub> – Q <sub>H</sub>	C <sub>OUT</sub>	-	High-Impedance Output State	15	15	15	pF
Power Dissipation Capacitance <sup>7</sup>	C <sub>PD</sub>	-	T <sub>J</sub> = 25°C, V <sub>CC</sub> = 5.0V	TYPICAL			pF
				300			

7. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

## Timing Requirements<sup>6</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>5</sup>	
Minimum Setup Time, SER to SRCLK (Figure 5)	t <sub>SU</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	50	65	75	ns
		3.0V		40	50	60	
		4.5V		10	13	15	
		6.0V		9	11	13	
Minimum Setup Time, SRCLK to RCLK (Figure 6)	t <sub>SU</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	75	95	110	ns
		3.0V		60	70	80	
		4.5V		15	19	22	
		6.0V		13	16	19	





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## Timing Requirements<sup>6</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>5</sup>	
Minimum Hold Time, SRCLK to SER (Figure 5)	t <sub>h</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	5	5	5	ns
		3.0V		5	5	5	
		4.5V		5	5	5	
		6.0V		5	5	5	
Minimum Recovery Time, SRCLR to SRCLK (Figure 2)	t <sub>rec</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	50	65	75	ns
		3.0V		40	50	60	
		4.5V		10	13	15	
		6.0V		9	11	13	
Minimum Pulse Width, SRCLR (Figure 2)	t <sub>w</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	60	75	90	ns
		3.0V		45	60	70	
		4.5V		12	15	18	
		6.0V		10	13	15	
Minimum Pulse Width, SRCLK (Figure 1)	t <sub>w</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	50	65	75	ns
		3.0V		40	50	60	
		4.5V		10	13	15	
		6.0V		9	11	13	
Minimum Pulse Width, RCLK (Figure 6)	t <sub>w</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	50	65	75	ns
		3.0V		40	50	60	
		4.5V		10	13	15	
		6.0V		9	11	13	
Maximum Input Rise and Fall Times, (Figure 1)	t <sub>r</sub> , t <sub>f</sub>	2.0V	Input t <sub>r</sub> = t <sub>f</sub> = 6ns	1000	1000	1000	ns
		3.0V		800	800	800	
		4.5V		500	500	500	
		6.0V		400	400	400	

## Switching Waveforms

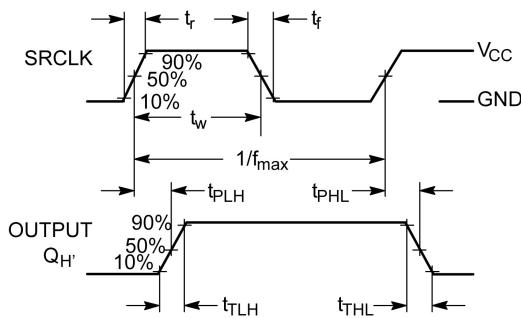


Figure 1 – Clock Propagation Delay & Output Timing

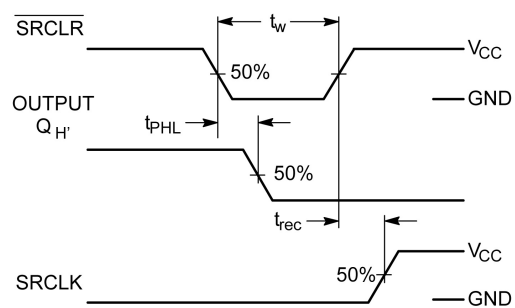


Figure 2 – Reset Propagation Delay & Timing





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## Switching Waveforms continued

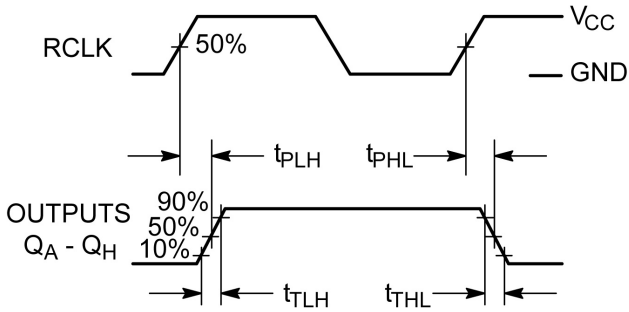


Figure 3 – Clock Propagation Delay & Output Timing

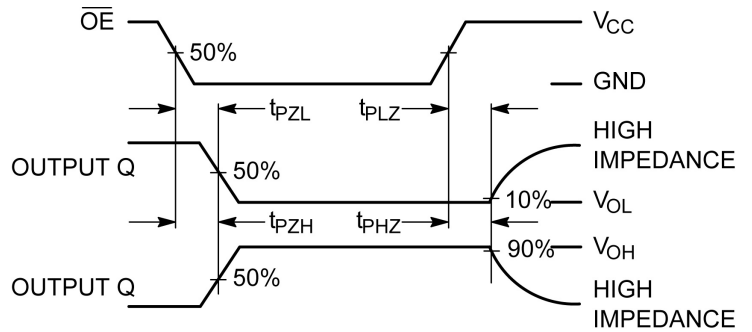


Figure 4 – Enable to Output Propagation Delay

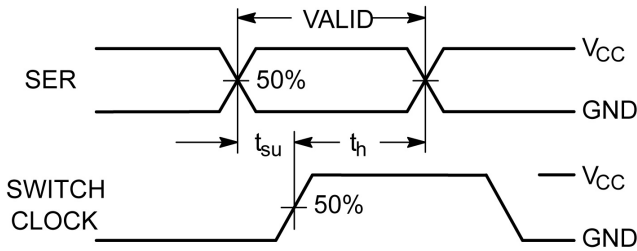


Figure 5 – Data Transition Timing, Serial Input & Clock

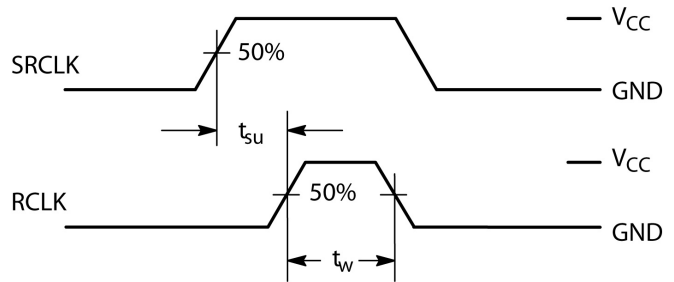
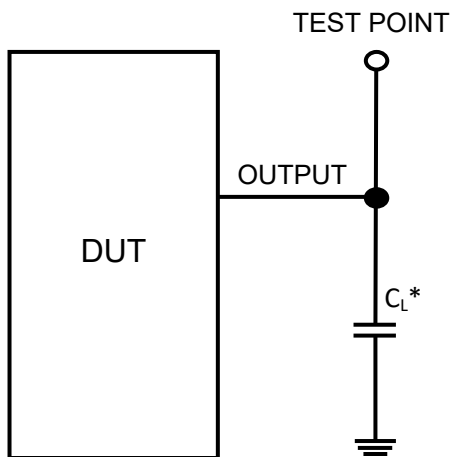
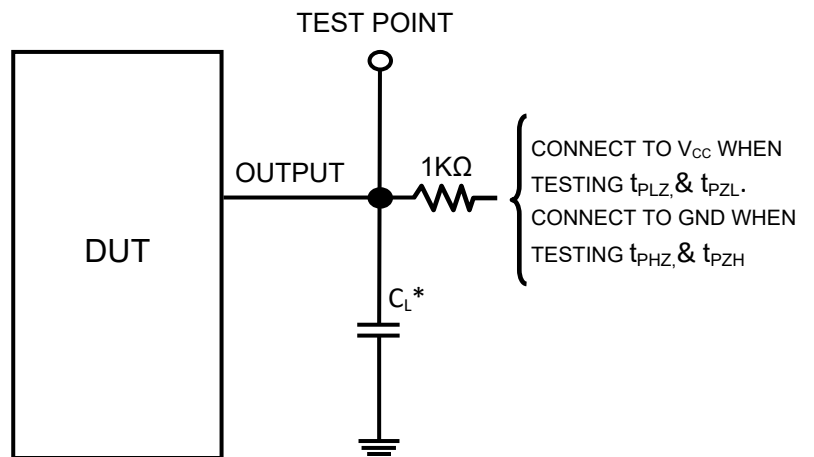


Figure 6 – Shift Clock to Register Clock Setup Timing



\* Includes all probe and jig capacitance

Figure 7 – Test Setup



\* Includes all probe and jig capacitance

Figure 8 – Test Setup



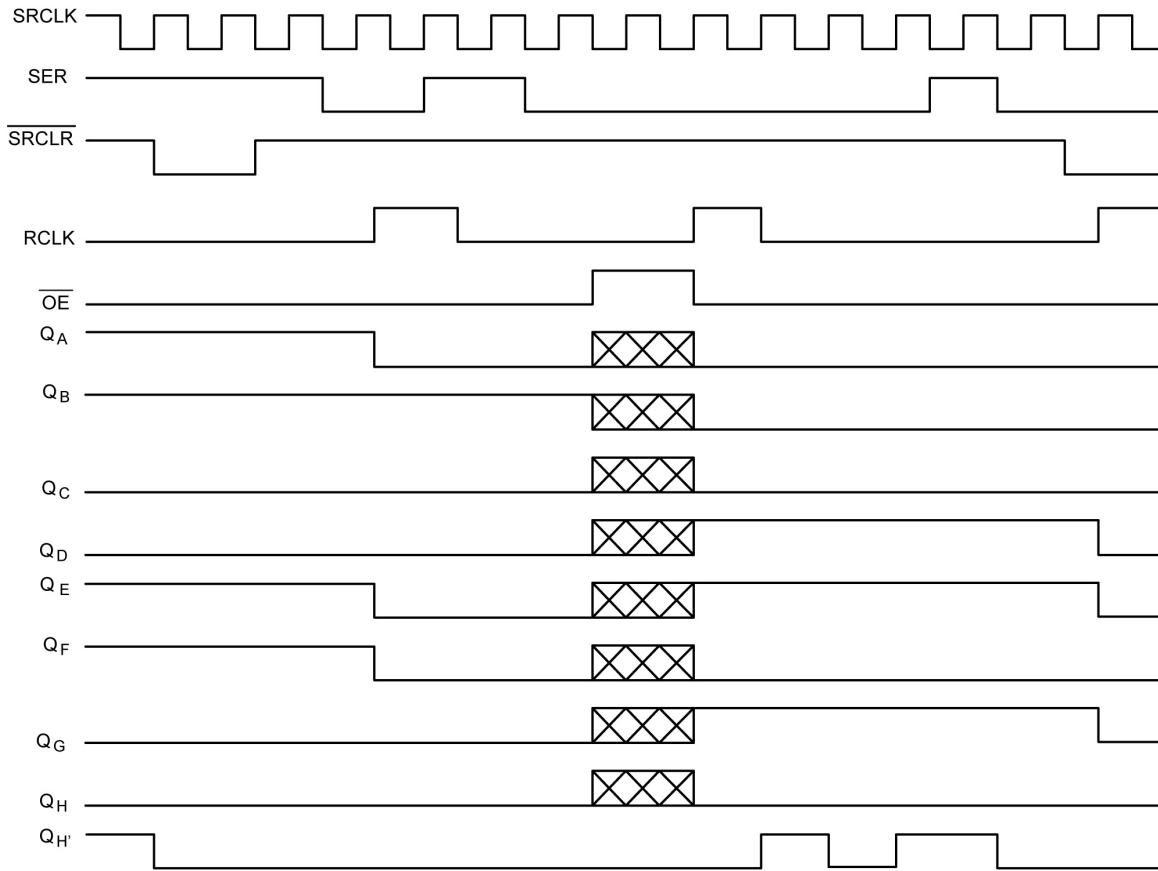




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## Timing Diagram



NOTE: **XXXX** implies that the output is in a high-impedance state

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