High Speed CMOS Logic – 54HC30

8-Input NAND Gate Logic IC in bare die form

Rev 1.0
7/5/2019

Description

The 54HC30 8-Input NAND Gate is made using a 2.5µm 5V CMOS process & combines the high speed of LSTTL with CMOS low power consumption. The device performs Boolean functions in positive logic:
$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$ or
$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$.
Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. Internal circuitry comprises 3 stages & includes buffered output for high noise immunity & stability.

Features:

- Low Input Current: 1µA
- Output Drive Capability: 10 LSTTL loads
- Outputs Directly Interface to CMOS, NMOS, & TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS30
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

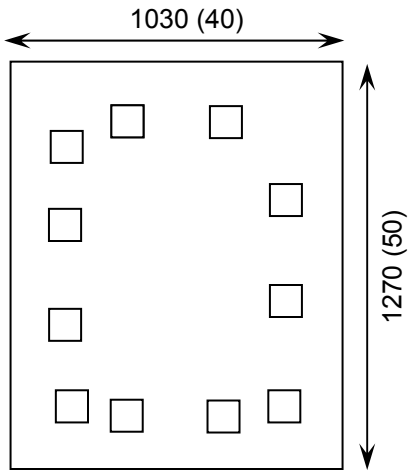
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1030 x 1270 40 x 50	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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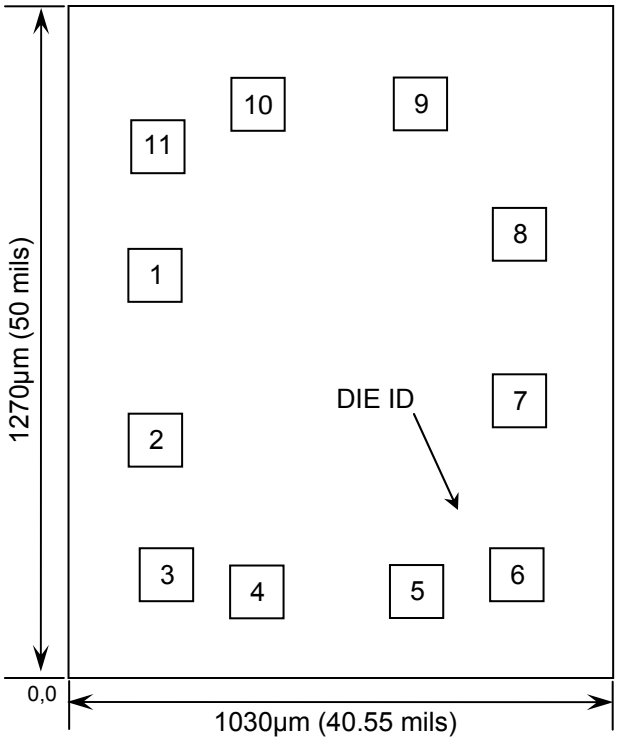
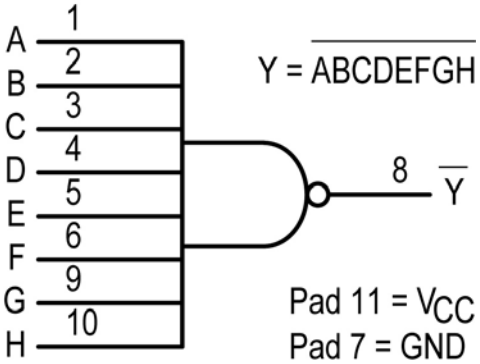
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A	0.1155	0.7200
2	B	0.1155	0.4015
3	C	0.1355	0.1465
4	D	0.3080	0.1160
5	E	0.6220	0.1160
6	F	0.8130	0.1465
7	GND	0.8130	0.4810
8	$\overline{Y}$	0.8130	0.8000
9	G	0.6220	1.0465
10	H	0.3080	1.0465
11	V_{CC}	0.1155	0.9670
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Function Table

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = High level (steady state)
L = Low level (steady state)
X = don't care

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-55	+125	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2.0V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6V	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	

4. -55°C ≤ T_J ≤ +125°C

DC Electrical Characteristics Continued (Voltages referenced to GND)

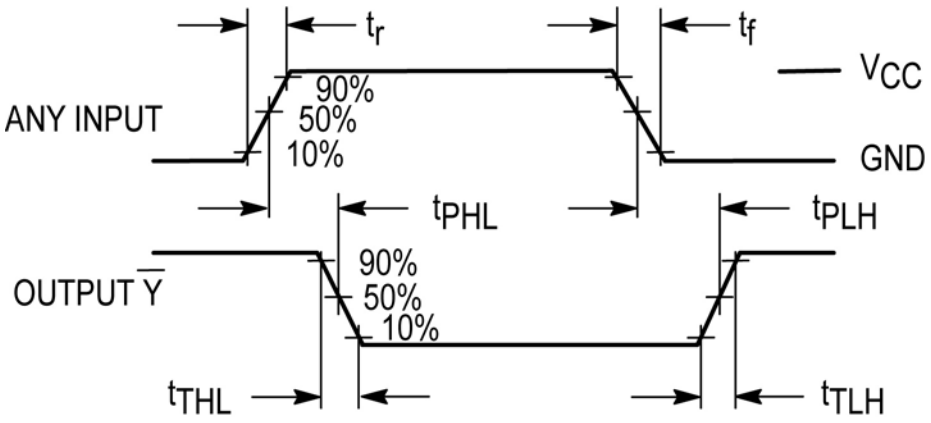
PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	2V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 4.0mA$	3.98	3.84	3.70	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 5.2mA$	5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V_{OL}	2V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 4.0mA$	0.26	0.33	0.40	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 5.2mA$	0.26	0.33	0.40	V
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	2	20	40	µA

AC Electrical Characteristics[5]

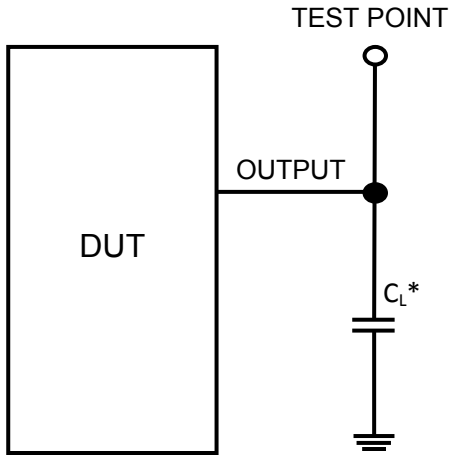
PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Any Input to Output Y	t_{PLH}, t_{PHL}	2V	$C_L = 50pF$, $t_r = t_f = 6ns$	175	220	265	ns
		4.5V		35	44	53	
		6.0V		30	37	45	
Maximum Output Rise and Fall Time, Any Output	t_{TLH}, t_{THL}	2V	$C_L = 50pF$, $t_r = t_f = 6ns$	75	95	110	ns
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[6]	C_{PD}	-	$T_J = 25°C$, $V_{CC} = 5.0V$	TYPICAL			pF
				27			

5. Not production tested in die form, characterized by chip design and tested in package.
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance