High Speed CMOS Logic – 54HC244

Octal 3-State Non-Inverting Buffer / Line Driver / Line Receiver in bare die form

Rev 1.1
01/05/18

Description

The 54HC244 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. The device can be used as two 4-bit buffers or one 8-bit buffer and features non-inverting inputs with two output enables, each controlling four of the 3-state outputs. The device is specifically designed to improve performance and density in clock drivers, 3-state memory address drivers and bus orientated transmitters and receivers. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}

Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS244
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

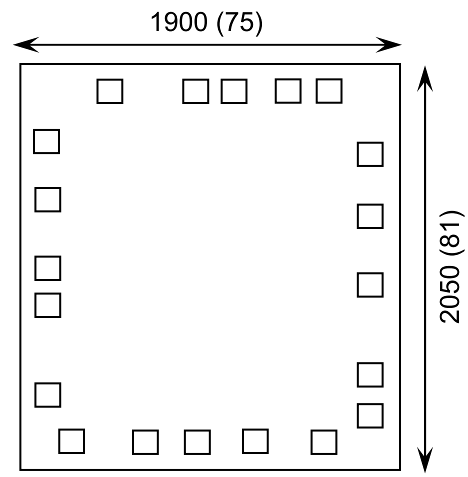
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



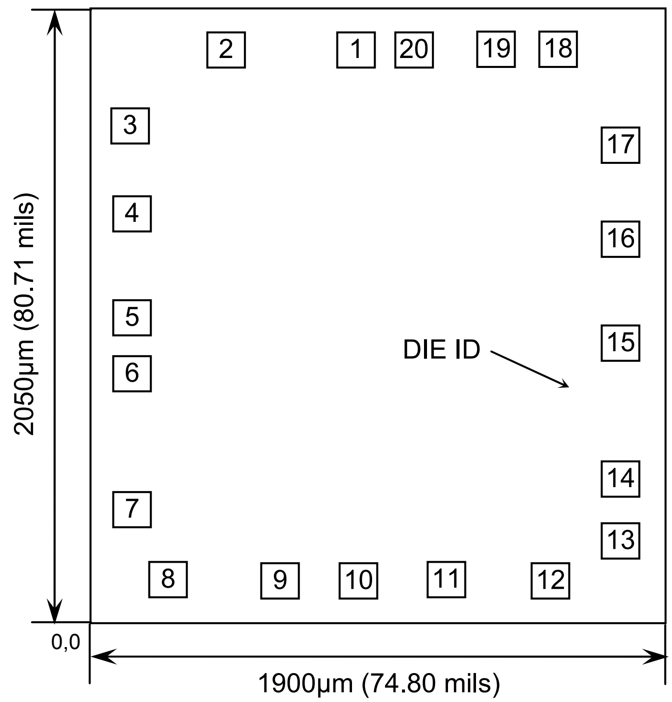
Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

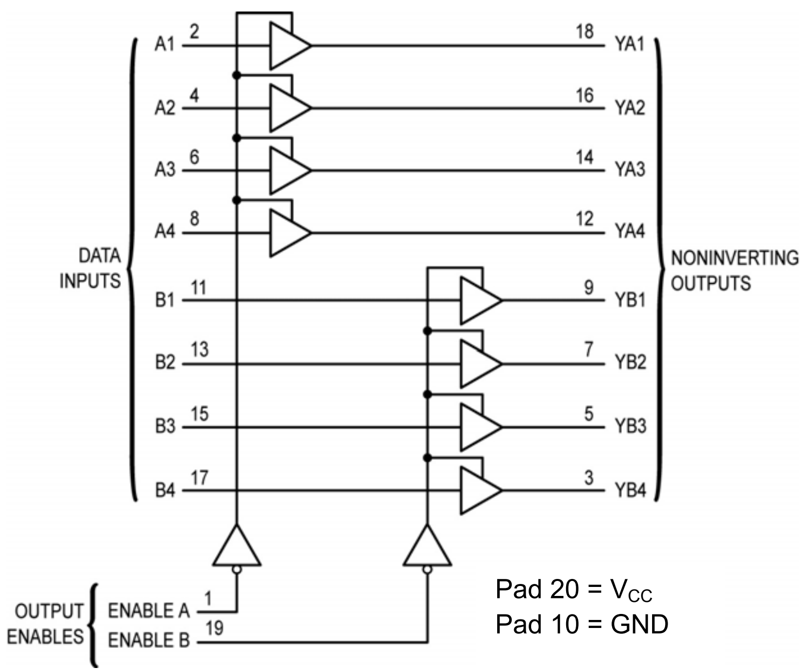
Die Size (Unsawn)	1900 x 2050 75 x 81	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions



PAD	FUNCTION
1	ENABLE A
2	A1
3	YB4
4	A2
5	YB3
6	A3
7	YB2
8	A4
9	YB1
10	GND
11	B1
12	YA4
13	B2
14	YA3
15	B3
16	YA2
17	B4
18	YA1
19	ENABLE B
20	V_{CC}
CONNECT CHIP BACK TO V_{CC} OR FLOAT	

Logic Diagram



Pad 20 = V_{CC}
Pad 10 = GND

Truth Table

INPUTS		OUTPUTS
ENABLE A ENABLE B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care
Z = High impedance

Pad Descriptions

ADDRESS INPUTS
A1, A2, A3, A4, B1, B2, B3, B4
(Pads 2, 4, 6, 8, 11, 13, 15, 17)
Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROL INPUTS
Enable A, Enable B (Pads 1, 19)
Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as non-inverting buffers. When a high level is applied, the outputs assume the high impedance state.

OUTPUTS
YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4
(Pads 18, 16, 14, 12, 9, 7, 5, 3)
Device outputs. Depending upon the state of the output– enable pins, these outputs are either non-inverting outputs or high–impedance outputs.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±35	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±75	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_A	-55	+125	°C
Input Rise and Fall Time	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS 25°C	LIMITS 85°C	LIMITS FULL RANGE[4]	UNITS
Minimum High-Level Input Voltage	V_{IH}	2.0V	$V_{OUT} = V_{CC}$ -0.1V, $\lvert I_{OUT} \rvert \le 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	$V_{OUT} = 0.1V$, $\lvert I_{OUT} \rvert \le 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	
Minimum High-Level Output Voltage	V_{OH}	2.0V	$V_{IN} = V_{IH}$, $\lvert I_{OUT} \rvert \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	$V_{IN} = V_{IH}$, $\lvert I_{OUT} \rvert \le 2.4mA$	2.48	2.34	2.2	V
		4.5V	$V_{IN} = V_{IH}$, $\lvert I_{OUT} \rvert \le 6.0mA$	3.98	3.84	3.70	
		6.0V	$V_{IN} = V_{IH}$, $\lvert I_{OUT} \rvert \le 7.8mA$	5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert \le 2.4mA$	0.26	0.33	0.40	V
		4.5V	$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert \le 6.0mA$	0.26	0.33	0.40	
		6.0V	$V_{IN} = V_{IL}$, $\lvert I_{OUT} \rvert \le 7.8mA$	0.26	0.33	0.40	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum 3-State leakage current	I_{OZ}	6.0V	$V_{OUT} = V_{CC}$ or 0, $V_{IN} = V_{IL}$ or V_{IH}	±0.5	±5.0	±10	μA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	4	40	160	μA

4. −55˚C ≤ T_J ≤ +125˚C

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, A to YA or B to YB (Figure 1, 3)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	96	115	135	ns
		3.0V		50	60	70	
		4.5V		18	23	27	
		6.0V		15	20	23	
Maximum Propagation Delay, Output Enable to YA or YB (Figure 2,4)	t_{PLZ}, t_{PHZ}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	110	140	165	ns
		3.0V		60	70	80	
		4.5V		22	28	33	
		6.0V		19	24	28	
Maximum Propagation Delay, Output Enable to YA or YB (Figure 2,4)	t_{PZL}, t_{PZH}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	110	140	165	ns
		3.0		60	70	80	
		4.5V		22	28	33	
		6.0V		19	24	28	
Maximum Output Rise and Fall Time (Figure 1, 3)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	60	75	90	ns
		3.0V		23	27	32	
		4.5V		12	15	18	
		6.0V		10	13	15	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Maximum Three-State Output Capacitance (Output in High-Impedance State)	C_{OUT}	-	-	15	15	15	pF
Power Dissipation Capacitance (Per Buffer)[5]	C_{PD}	-	T_A = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				34			

5. Not production tested in die form, characterized by chip design and tested in package LAT.
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveforms

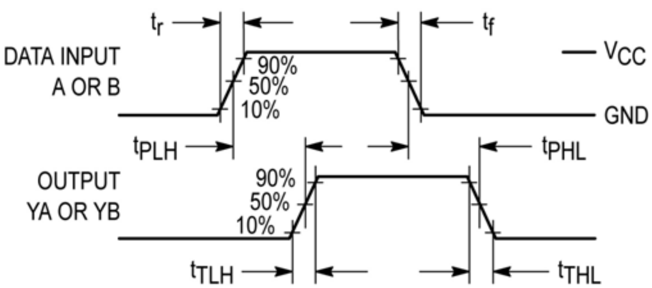


Figure 1 – Propagation Delay
Input A or B to Output YA or YB

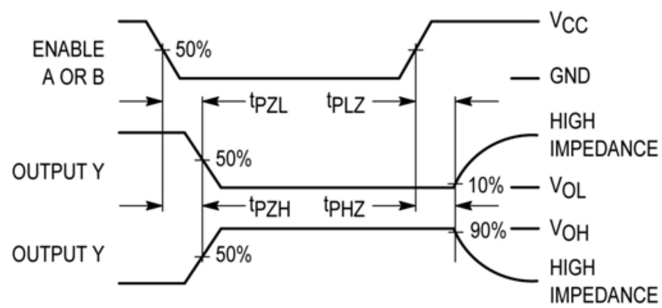
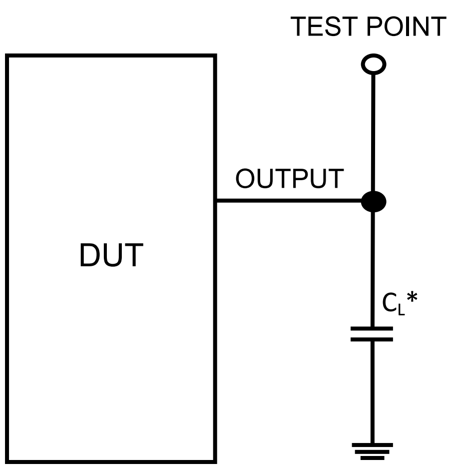


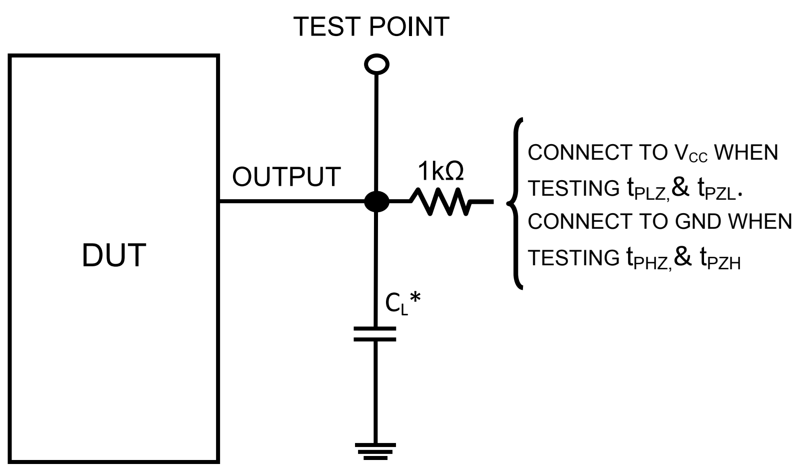
Figure 2 – Propagation Delay
Output Enable to Output YA or YB

Test Circuits



* Includes all probe and jig capacitance

Figure 3



* Includes all probe and jig capacitance

Figure 4